KENWOOD®

STEREO FOR YOUR CAR

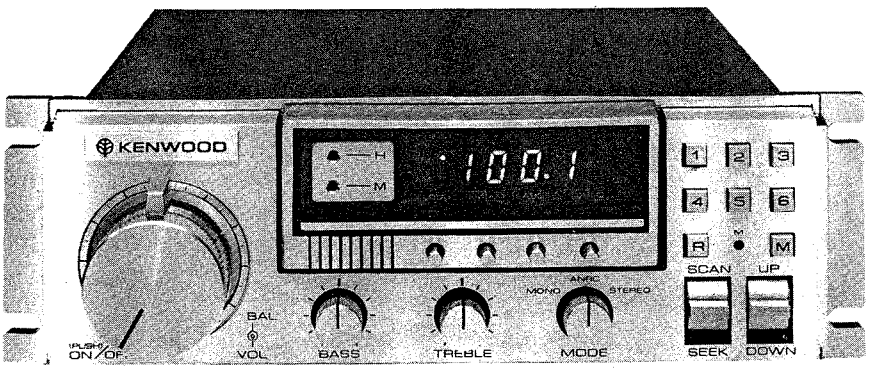
SERVICE MANUAL

KTC-767

An item of adjustment is written in three languages — English, French and German.

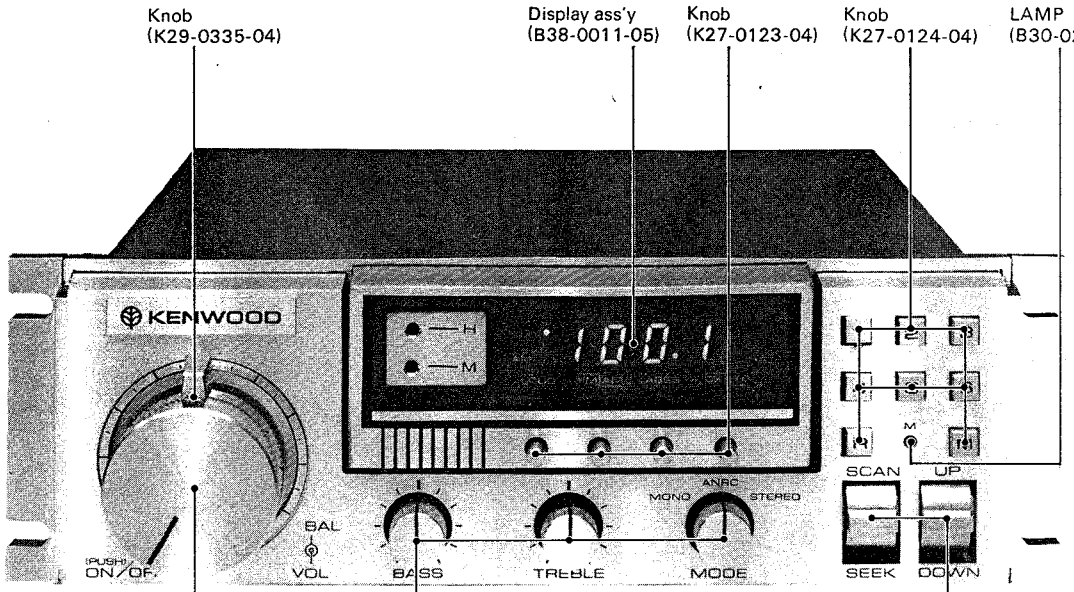
Un article sur réglages est écrit en trois langues, Anglais, Français et Allemand.

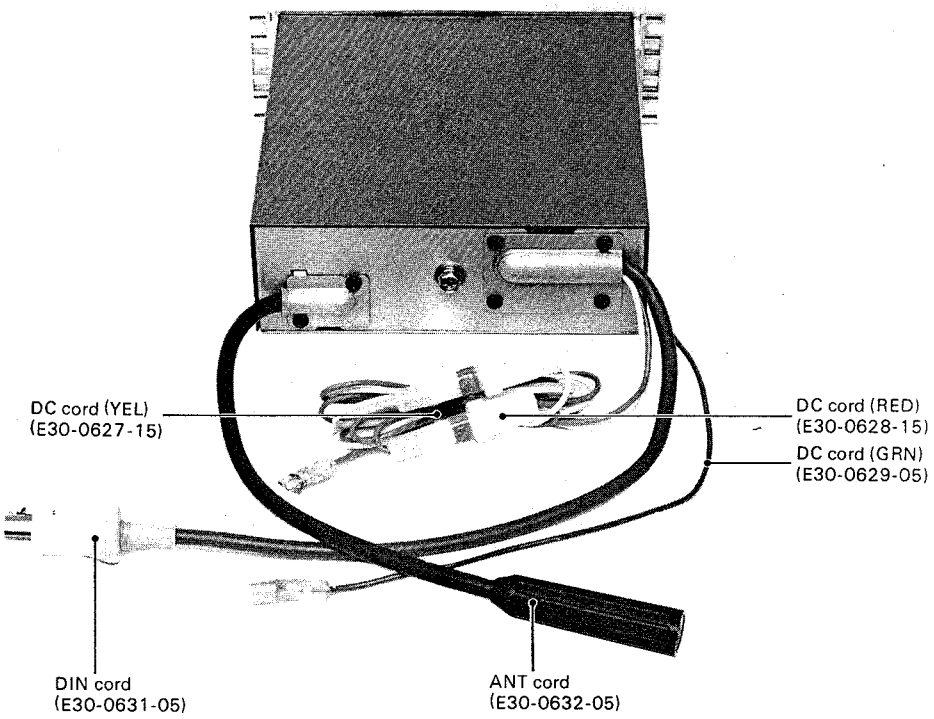
Ein Artikel der Abgleich wird auf drei Sprachen, Englische, Französisch und Deutsch geschrieben.



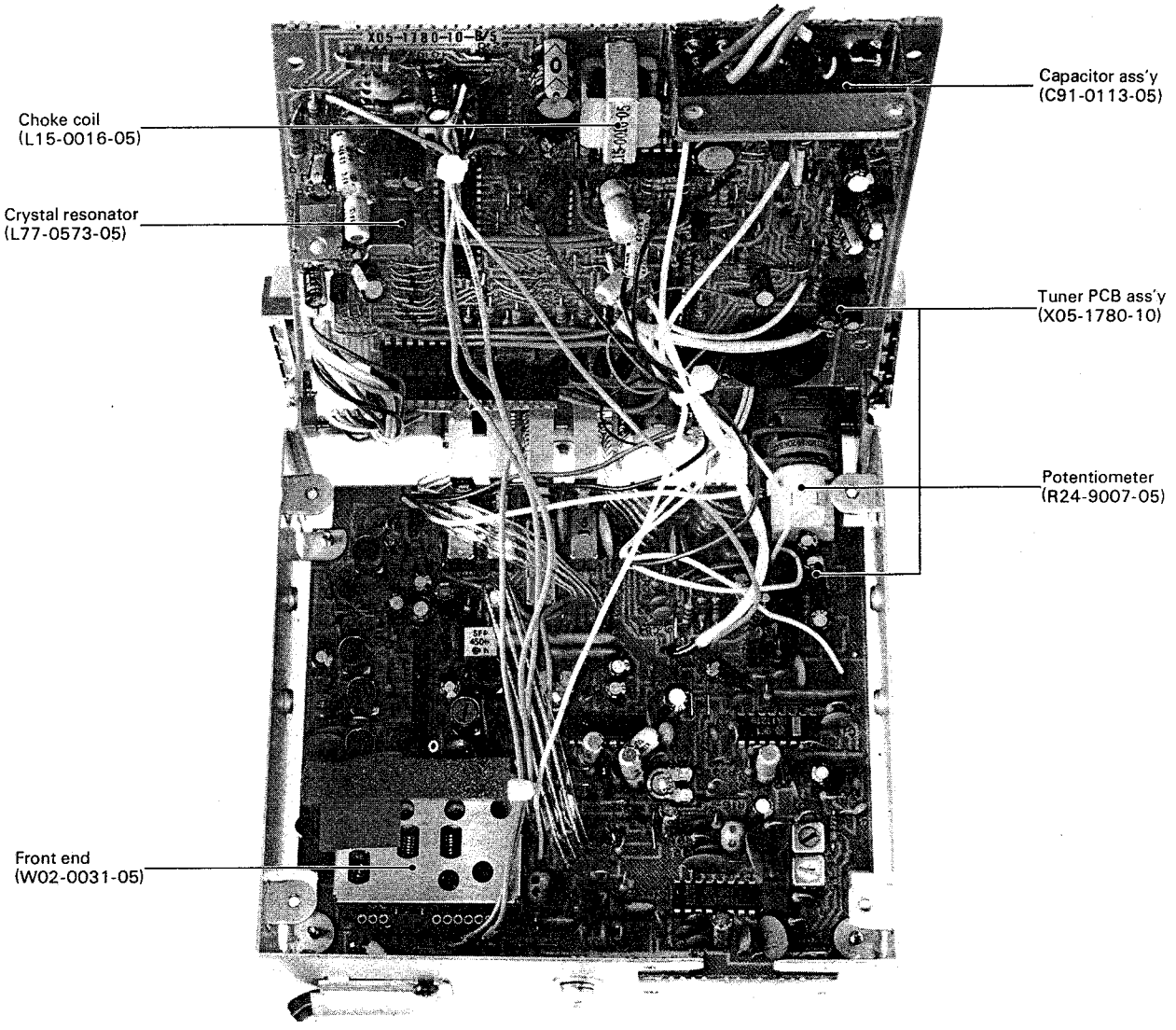
SYNTHESIZER TUNER

EXTERNAL VIEW





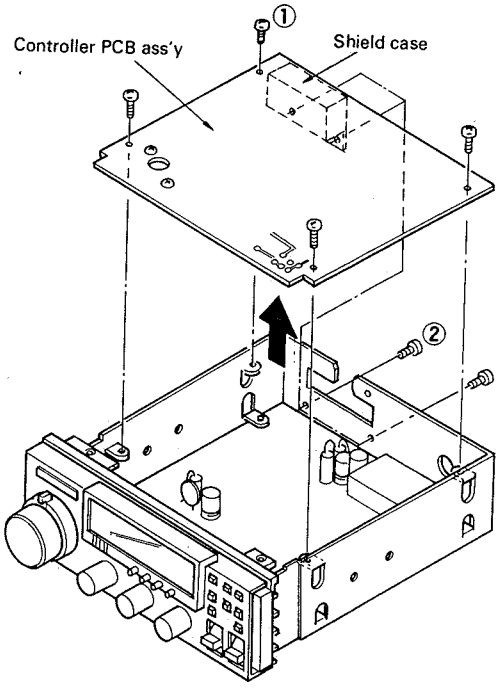
INTERNAL VIEW



DISASSEMBLY FOR REPAIR

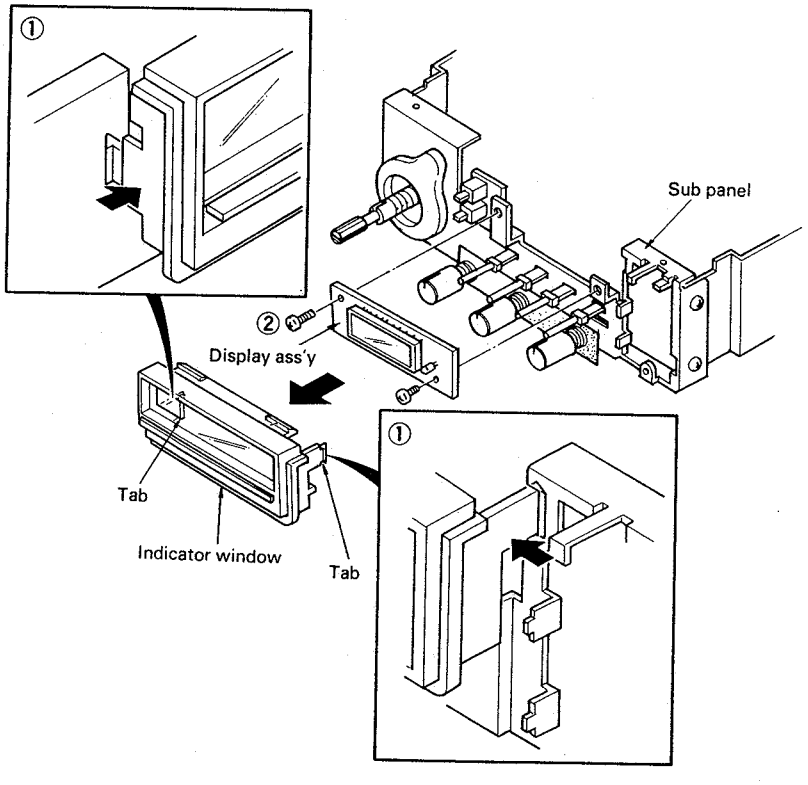
CONTROLLER PCB ASS'Y DETACHMENT

① Remove the four screws from the sub chassis.
② Remove the two screws from the shield case.



DISPLAY ASS'Y DETACHMENT

① Remove the indicator window by pressing the tab inwards gently from the sub chassis.
② Remove the two screws from the sub panel.

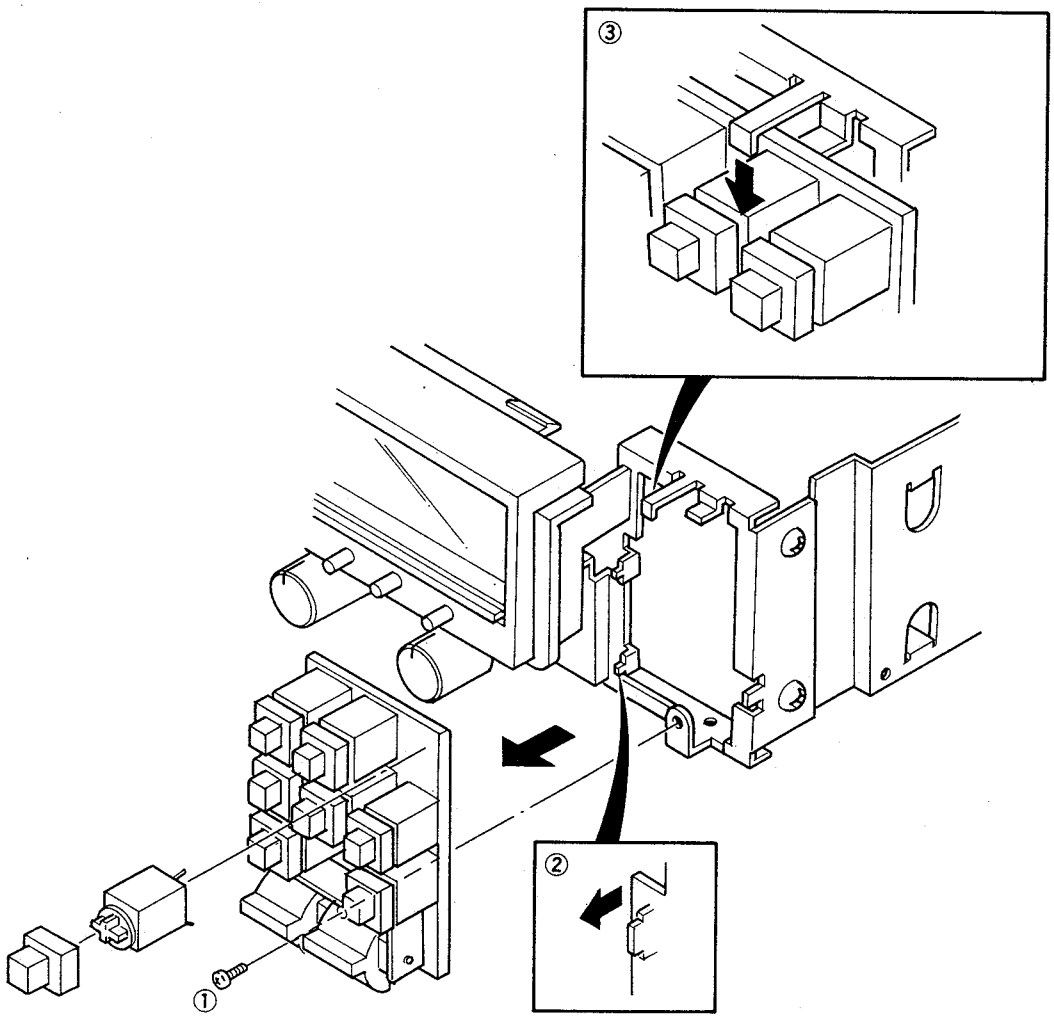


DISASSEMBLY FOR REPAIR

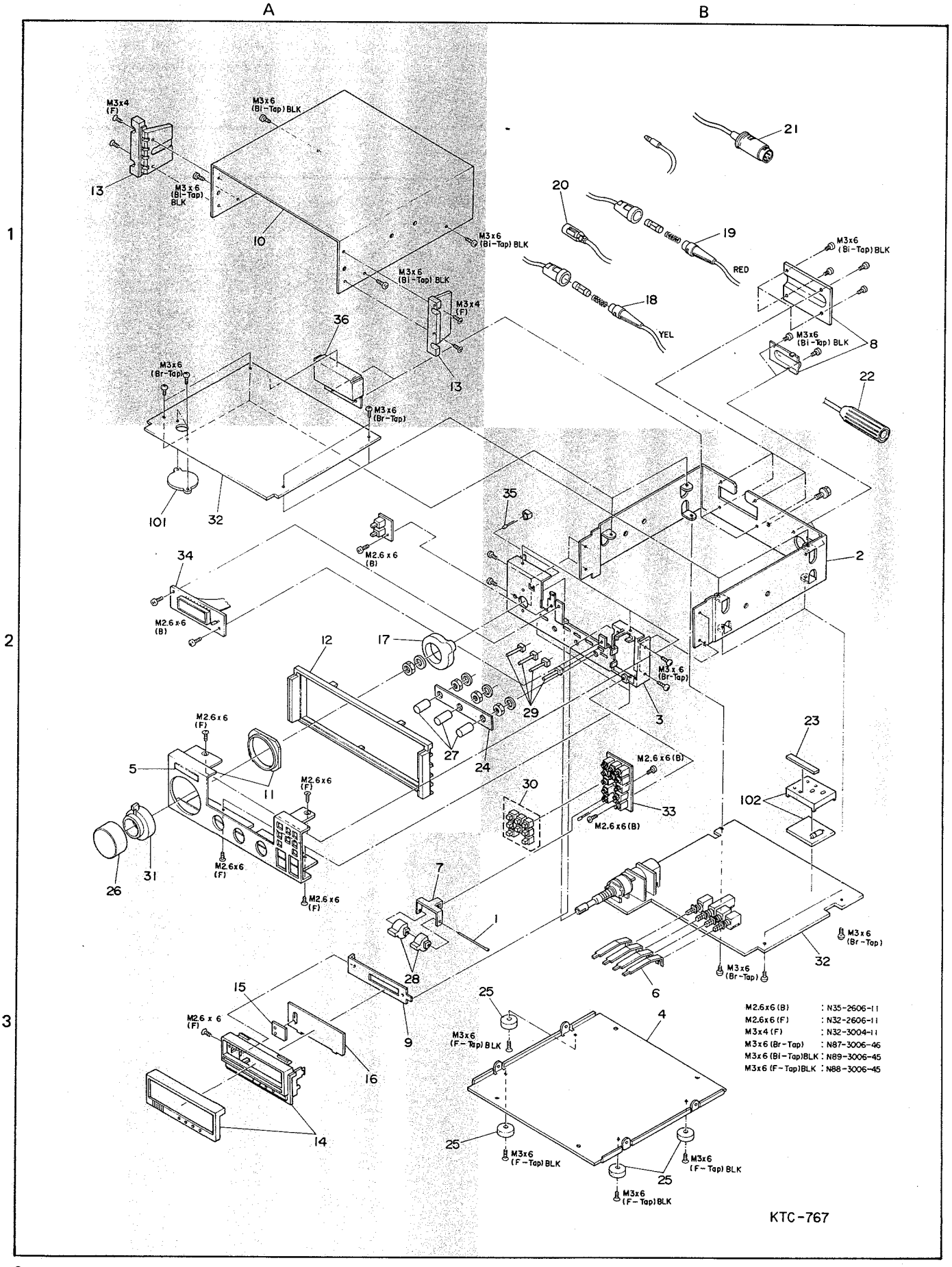
SWITCH PCB ASS'Y DETACHMENT

① Remove the screw from the sub panel.
② Pull the switch PCB ass'y from the sub panel.
③ Slide the switch PCB ass'y downwards.

When removing the switch, unsolder the leads of the switch from the foil side of the PCB.



EXPLODED VIEW



M2.6x6 (B)	: N35-2606-11
M2.6x6 (F)	: N32-2606-11
M3x4 (F)	: N32-3004-11
M3x6 (Br-Tap)	: N87-3006-46
M3x6 (Bi-Tap)BLK	: N89-3006-45
M3x6 (F-Tap)BLK	: N88-3006-45

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ADJUSTMENT

NO.	ALIGNMENT	TEST EQUIPMENTS		TUNER SETTING	OUTPUT INDICATOR	ADJUSTMENT POINTS	REMARKS
		CONNECTION	SETTING				
FM							
1	IFT	Ⓐ	100.1 MHz 1 kHz (Mod) 75 kHz (Dev) 20 dB (75Ω)	100.1 MHz MONO	TP1	T2	Minimum distortion
2a	DISCRIMI-NATOR	Ⓐ	100.1 MHz 1 kHz (Mod) 75 kHz (Dev) 80 dB (75Ω)	- ditto -	TP2 ⓐ	L5	0V
2b	DISCRIMI-NATOR	Ⓐ	- ditto -	- ditto -	TP1	L6	Minimum distortion
3	VCO	Ⓐ	- ditto -	100.1 MHz STEREO	TP3 ⓑ	VR1	19 kHz
4	SEPARATION	Ⓑ	100.1 MHz 1 kHz (Mod) 68.25 kHz (Mod) L or R (SELECTOR)	- ditto -	TP1	VR2	Minimum crosstalk
AM							
1	FREQUENCY CALIBRATION	Ⓒ	1620 kHz 400 Hz, 30% 80 dB (75Ω)	1620 kHz	TP4 ⓒ	L8	7.5V
2a	TRACKING	Ⓒ	600 kHz 400 Hz, 30% 20 dB (75Ω)	600 kHz	TP1	L7, 9	Maximum deflection
2b	TRACKING	Ⓒ	1400 kHz 400 Hz, 30% 20 dB (75Ω)	1400 kHz	- ditto -	TC1,2	- ditto -
3	IFT	Ⓒ	1000 kHz 400 Hz, 30% 20 dB (75Ω)	1000 kHz	- ditto -	L10, 11	- ditto -
4	STOP SIGNAL	Ⓒ	- ditto -	- ditto -	TP5 ⓓ	L12	Minimum deflection (4V → 0.6V)

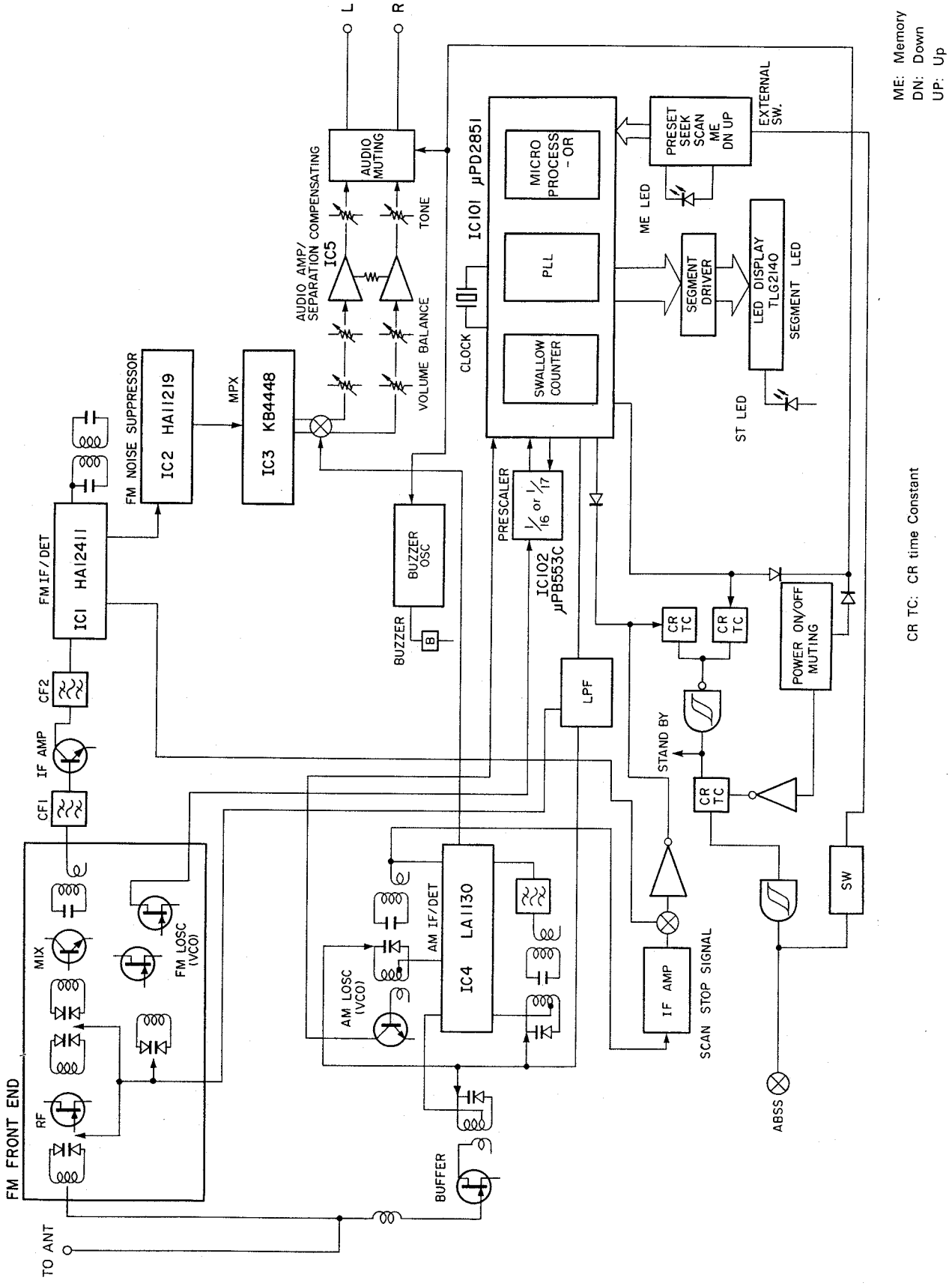
Note 1:
Set the FM-SG frequency to the 100.1 MHz accurately with a frequency counter or marker oscillator.

Note 2:
Set the AM-SG frequency to be the desired frequency accurately with a frequency counter or marker oscillator. If your local station is broadcasting with a frequency close to 600, 1000 or 1400 kHz, receive this signal for tracking and IFT alignment.

Note 3:
The front end section has already been completely adjusted in the factory and further adjustment is not necessary.
If the ceramic trimmers or the coils are accidentally moved, perform the following adjustment.

1) If the ceramic trimmers have been moved:
   1. Set FM-SG to 104.1 MHz, 1 kHz Mod., ±75 kHz Dev. and connect it to the antenna terminal of the tuner.
   2. Set the LED Display at 104.1 MHz.
   3. Adjust TC1 and TC2 so that maximum output is obtained.
2) If the coils have been moved:
   1. Set FM-SG to 90.1 MHz, 1 kHz Mod., ±75 kHz Dev. and connect it to the antenna terminal of the tuner.
   2. Set the LED Display at 90.1 MHz.
   3. Adjust the coil pitch of L1, 3 and 4 with a screwdriver or the like so that maximum output is obtained.

BLOCK DIAGRAM



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RÉGLAGE

N°	ALIGNEMENT	APPAREILLAGE		RÉGLAGE DU TUNER	INDICATEUR DE SORTIE	POINTS DE RÉGLAGES	REMARQUES
		RACCORDEMENT	RÉGLAGE				
FM							
1	TFI	Ⓐ	100,1 MHz 1 kHz (Mod) 75 kHz (Dév) 20 dB (75Ω)	100,1 MHz MONO	TP1	T2	Distorsion minimale
2a	DISCRIMI-NATEUR	Ⓐ	100,1 MHz 1 kHz (Mod) 75 kHz (Dév) 80 dB (75Ω)	- idem -	TP2 ⓐ	L5	0V
2b	DISCRIMI-NATEUR	Ⓐ	- idem -	- idem -	TP1	L6	Distorsion minimale
3	VCO	Ⓐ	- idem -	100, 1 MHz STEREO	TP3 ⓑ	VR1	19 kHz
4	SÉPARATION	Ⓑ	100,1 MHz 1 kHz (Mod) 68,25 kHz (Dév) L or R (Sélecteur)	- idem -	TP1	VR2	Diaphonic minimale
MA							
1	VOLTAGE DE PRÉRÉGLAGE	Ⓒ	1620 kHz 400 Hz, 30% 80 dB (75Ω)	1620 kHz	TP4 ⓒ	L8	7,5V
2a	ALIGNEMENT	Ⓒ	600 kHz 400 Hz, 30% 20 dB (75Ω)	600 kHz	TP1	L7, 9	Déviation maximale
2b	ALIGNEMENT	Ⓒ	1400 kHz 400 Hz, 30% 20 dB (75Ω)	1400 kHz	- idem -	TC1,2	- idem -
3	TFI	Ⓒ	1000 kHz 400 Hz, 30% 20 dB (75Ω)	1000 kHz	- idem -	L10, 11	- idem -
4	SIGNAL DE ARRÊT	Ⓒ	- idem -	- idem -	TP5 ⓓ	L12	Déviation minimale (4V → 0,6V)

Remarque 1.
Par le compteur de fréquence ou par l'oscillateur étalon, réglez la fréquence FM-SG à 100,1 MHz.

Remarque 2.
Par le compteur de fréquence ou par l'oscillateur étalon, réglez la fréquence AM-SG. Lorsqu'il y a une station émettrice locale ayant une de ces fréquences, vous pourrez régler en captant les émissions de cette station.

Remarque 3.
La tête RF a déjà été complètement ajustée en usine et aucun ajustement ultérieur n'est requis. Si les condensateurs d'antenne céramiques ou les selfs sont déplacées accidentellement, procéder alors aux réglages suivants:

1) Dans le cas où les condensateurs d'antenne céramiques auraient été déplacés.
   1. Régler FM-SG à 104,1 MHz, 1 kHz Mod., ±75 kHz Dev. et le connecter à la borne d'antenne du tuner.
   2. Régler l'exposition du LED à 104,1 MHz.
   3. Ajuster TC1 et TC2 de façon à obtenir la sortie maximale.
2) Si les selfs ont été déplacées:
   1. Régler FM-SG à 90,1 MHz, 1 kHz Mod., ±75 kHz Dev. et le connecter à la borne d'antenne du tuner.
   2. Régler l'exposition du LED à 90,1 MHz.
   3. Ajuster le pas de la self de L1, 3 et 4 avec un tournevis ou outil semblable de façon à obtenir la sortie maximale.

ABGLEICH

NR.	ABGLEICH	PRÜFEINRICHTUNG		TUNER EINSTELLUNG	AUSGANGS-ANZEIGE	EINSTELL-PUNKT	BEMERKUNGEN
		ANSCHLÜSSE	EINSTELLUNG				
UKW-EMPFANGSABTEILUNG							
1	ZF-T	Ⓐ	100,1 MHz 1 kHz ±75 kHz (Hub) 20 dB (75Ω)	100,1 MHz MONO	TP1	T2	Minimaler Klirrfaktor
2a	DISKRI-MINATOR	Ⓐ	100,1 MHz 1 kHz ±75 kHz (Hub) 80 dB (75Ω)	- dito -	TP2 ⓐ	L5	0V
2b	DISKRI-MINATOR	Ⓐ	- dito -	- dito -	TP1	L6	Minimaler Klirrfaktor
3	SPANNUNGS-GEREGELTER OSZILLATOR	Ⓐ	- dito -	100,1 MHz STEREO	TP3 ⓑ	VR1	19 kHz
4	STEREO KANAL-TRENNUNG	Ⓑ	100,1 MHz 1 kHz ±68,25 kHz (Hub) Wähler: L oder R	- dito -	TP1	VR2	Minimaler Übersprechen
MW-EMPFANGSABTEILUNG							
1	VOREINGE-STELLTE SPANNUNG	Ⓒ	1620 kHz 400 Hz, 30% 80 dB (75Ω)	1620 kHz	TP4 ⓒ	L8	7,5V
2a	EMPFANGS-BEREICH	Ⓒ	600 kHz 400 Hz, 30% 20 dB (75Ω)	600 kHz	TP1	L7, 9	Maximaler Ausschlag
2b	EMPFANGS-BEREICH	Ⓒ	1400 kHz 400 Hz, 30% 20 dB (75Ω)	1400 kHz	- dito -	TC1,2	- dito -
3	ZF-T	Ⓒ	1000 kHz 400 Hz, 30% 20 dB (75Ω)	1000 kHz	- dito -	L10, 11	- dito -
4	EINHALT SIGNAL	Ⓒ	- dito -	- dito -	TP5 ⓓ	L12	Minimaler Ausschlag (4V → 0,6V)

Anmerkung 1:
Die UKW-Meßsenderfrequenz mit Hilfe eines Frequenzzählers oder Frequenzmarkenoszillators genau einstellen.

Anmerkung 2:
Die MW-Meßsenderfrequenz mit Hilfe eines Frequenzzählers oder Frequenzmarkenoszillators einstellen. Strahlt der Ortssender Sendungen mit einer Frequenz nahe 600, 1000 oder 1400 kHz aus, diese für die Einstellung empfangen.

Anmerkung 3:
Das Frontende wurde bereits im Werk vollständig eingestellt. Weitere Einstellung ist daher nicht nötig. Wenn die Keramiktrimmer oder die Spulen aus Versehen bewegt wurden, ist folgende Korrektur vorzunehemen:

1) Wenn die Keramiktrimmer bewegt wurden:
   1. Den UKW-Signalgenerator auf 104,1 MHz, 1 kHz Modulation und ±75 kHz Hub einstellen und mit der Antennenklemme des Tuners verbinden.
   2. Den Skalenzeiger auf 104,1 MHz stellen.
   3. TC1 und TC2 so einstellen, daß ein maximales Ausgangssignal erhalten wird.
2) Wenn die Spulen bewegt wurden:
   1. Den UKW-Signalgenerator auf 90,1 MHz, 1 kHz Modulation und ±75 kHz Hub einstellen und mit der Antennen klemme des Tuners verbinden.
   2. Den Skalenzeiger auf 90,1 MHz stellen.
   3. Den Nutenschritt von L1, 3 und 4 mit einem Schraubenzieher etc. so einstellen, daß ein maximales Ausgangssignal erhalten wird.

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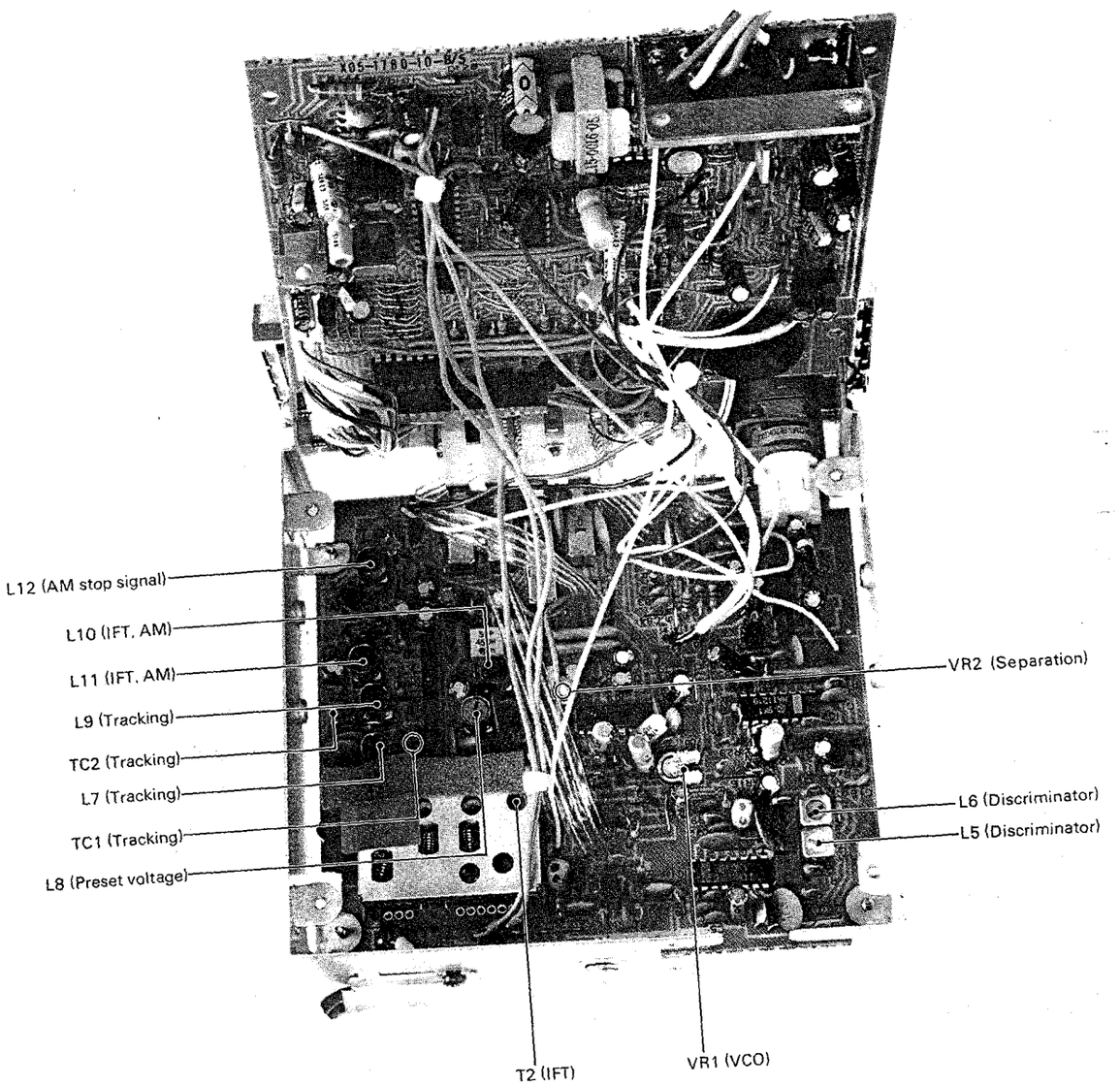
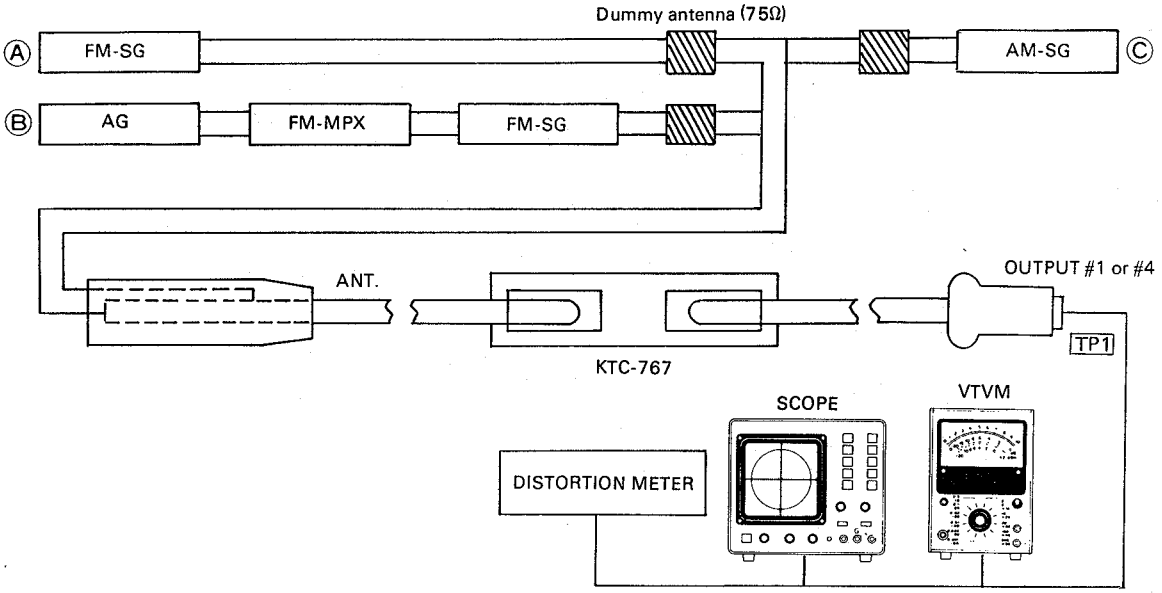
ADJUSTMENT/RÉGLAGES/ABGLEICH

PARTS LOCATION

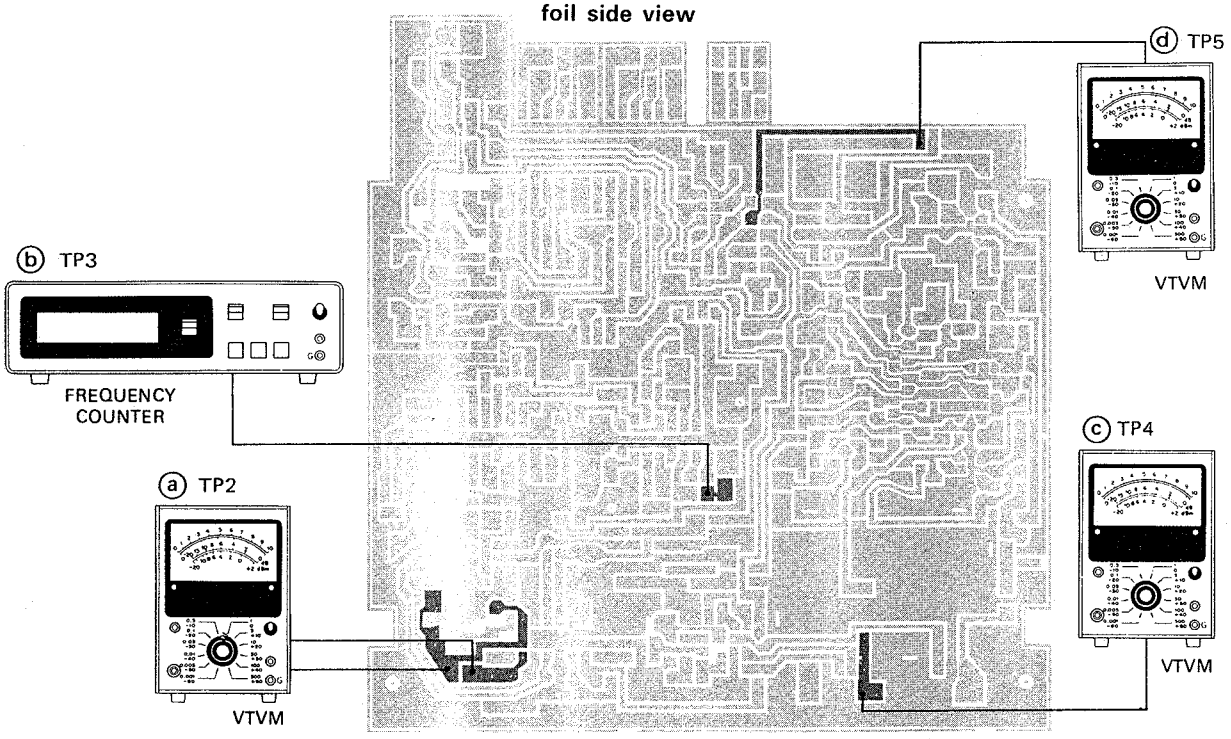


ADJUSTMENT/RÉGLAGES/ABGLEICH

TEST INSTRUMENTS	APPAREILLAGE	PRÜFINSTRUMENTE	
Oscilloscope	Oscilloscope	Oszilloskop	SCOPE
AM signal generator	Générateur MA	MW-Signalgenerator	AM-SG
FM signal generator	Générateur MF	UKW-Signalgenerator	FM-SG
Audio generator	Générateur audio fréquences	NF-Signalgenerator	AG
AC voltmeter	Voltmètre CA	Wechselspannungsmesser	VTVM
FM multiplex generator	Générateur multiplex stéréo	UKW-Multiplexgenerator	FM-MPX
Frequency counter	Fréquencemètre	Frequenzzähler	
DC voltmeter	Voltmètre CC	Gleichspannungsmesser	
Distortion meter	Distorsiomètre	Klirrfaktormesser	
Dummy antenna	Antenne fictive	Antennennachbildung	



PCB ASS'Y (X05-1780-10 A/5)
foil side view



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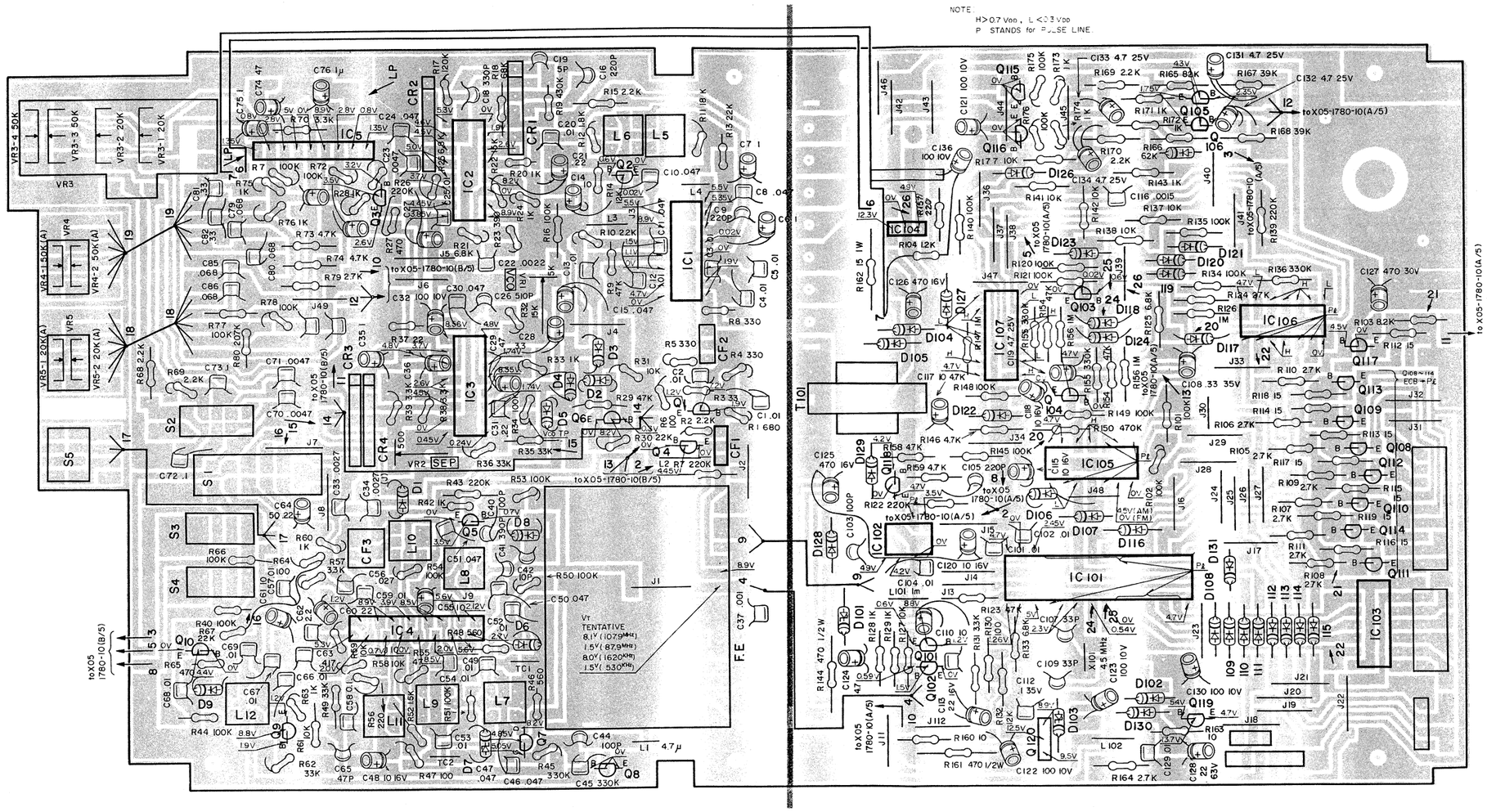
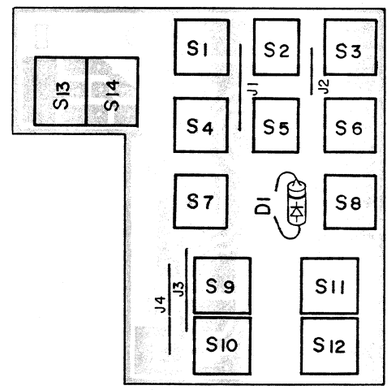
PC BOARD

TUNER (X05-1780-10) Components side view



Q101～106,119	:	2SC945 (Q,R)
Q108～116	:	2SC945 (P)
Q117,118	:	2SA733 (P)
Q120	:	2SD762 (P,Q)
IC101	:	μPD2851C
IC102	:	μPB553C
IC103	:	μPA53C
IC104	:	μPC7805H
IC105	:	μPD4081C (TC4081BP)
IC106	:	μPD4011C (TC4011BP)
IC107	:	μPD4069C (TC4069BP)
D101,102	:	WZ050
D103	:	WZ098
D104,105	:	W06B
D106～131	:	1SI555

SWITCH (X13-2720-10)



Q7	:	2SK193 (K,L)
Q5	:	2SC1675
Q2～4,6,8,10,11	:	2SC945 (R,Q)
D1～5	:	1SI555
D6～8	:	SVC321-3 (A,B)
D9	:	IN60
Q1,9	:	2SC1923
IC1	:	HA12411
IC2	:	HA11219
IC3	:	KB4448
IC4	:	LA1130
IC5	:	AN7311

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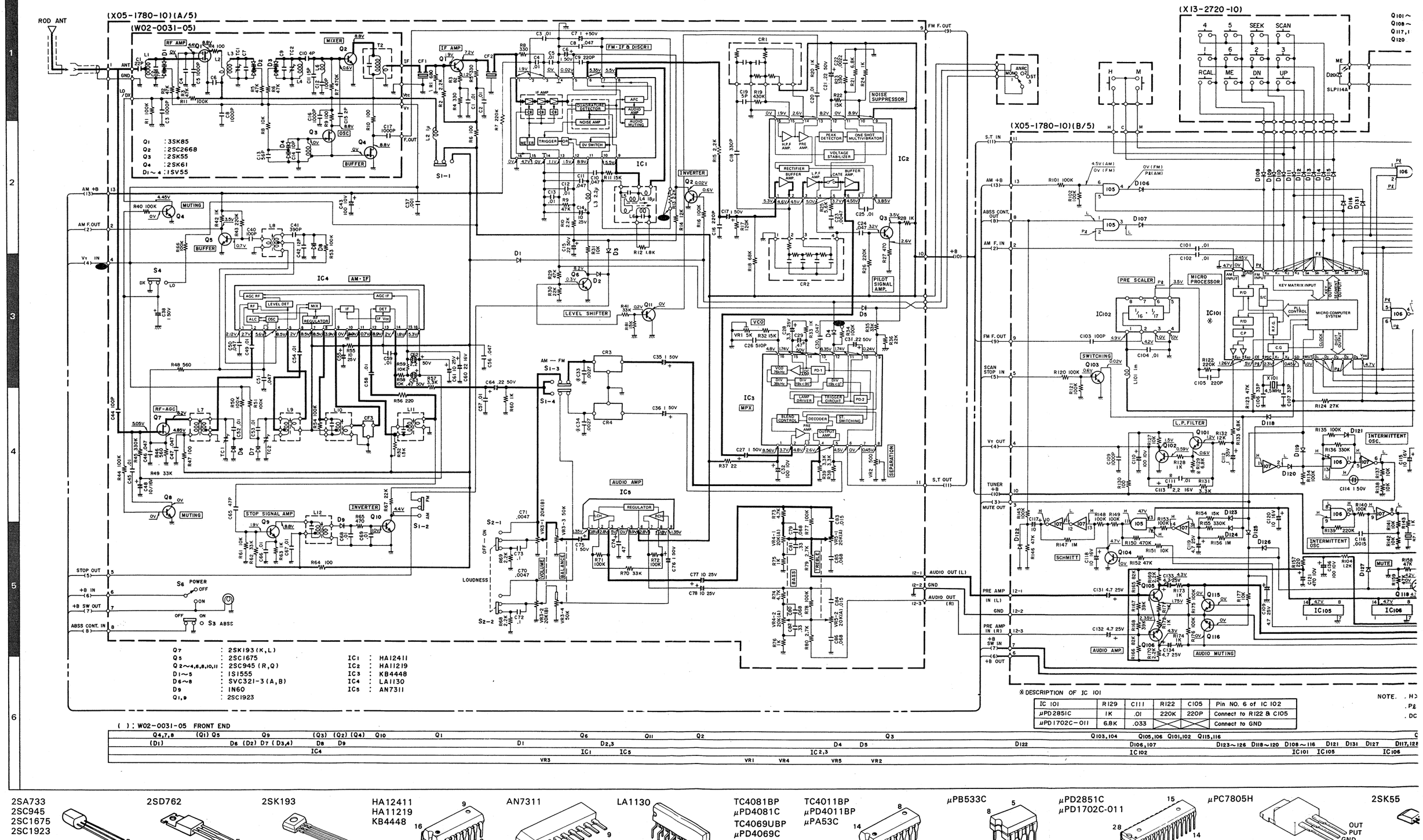
SYNTHESIZER TUNER



Q4,7,8	(Q1)	Q5	Q9	(Q3)	(Q2)	(Q4)	Q10	Q1	Q6	Q11	Q2	Q3	Q103,104	Q105,106	Q101,102	Q115,116	C
(D1)	D6 (D2) D7 (D3,4)		D8	D9	D1		D2,3		D4	D5	D122		D106,107		D123~126	D118~120	D108~116	D121	D131	D127	D117,128
IC4						IC1	IC5		IC2,3				IC102			IC101	IC105		IC106		
VR3								VR1	VR4	VR5	VR2										

2SA733
2SC945
2SC1675
2SC1923

2SD762

2SK193

HA12411
HA11219
KB4448

AN7311

LA1130

TC4081BP
μPD4081C
TC4069UBP
μPD4069C

TC4011BP
μPD4011BP
μPA53C

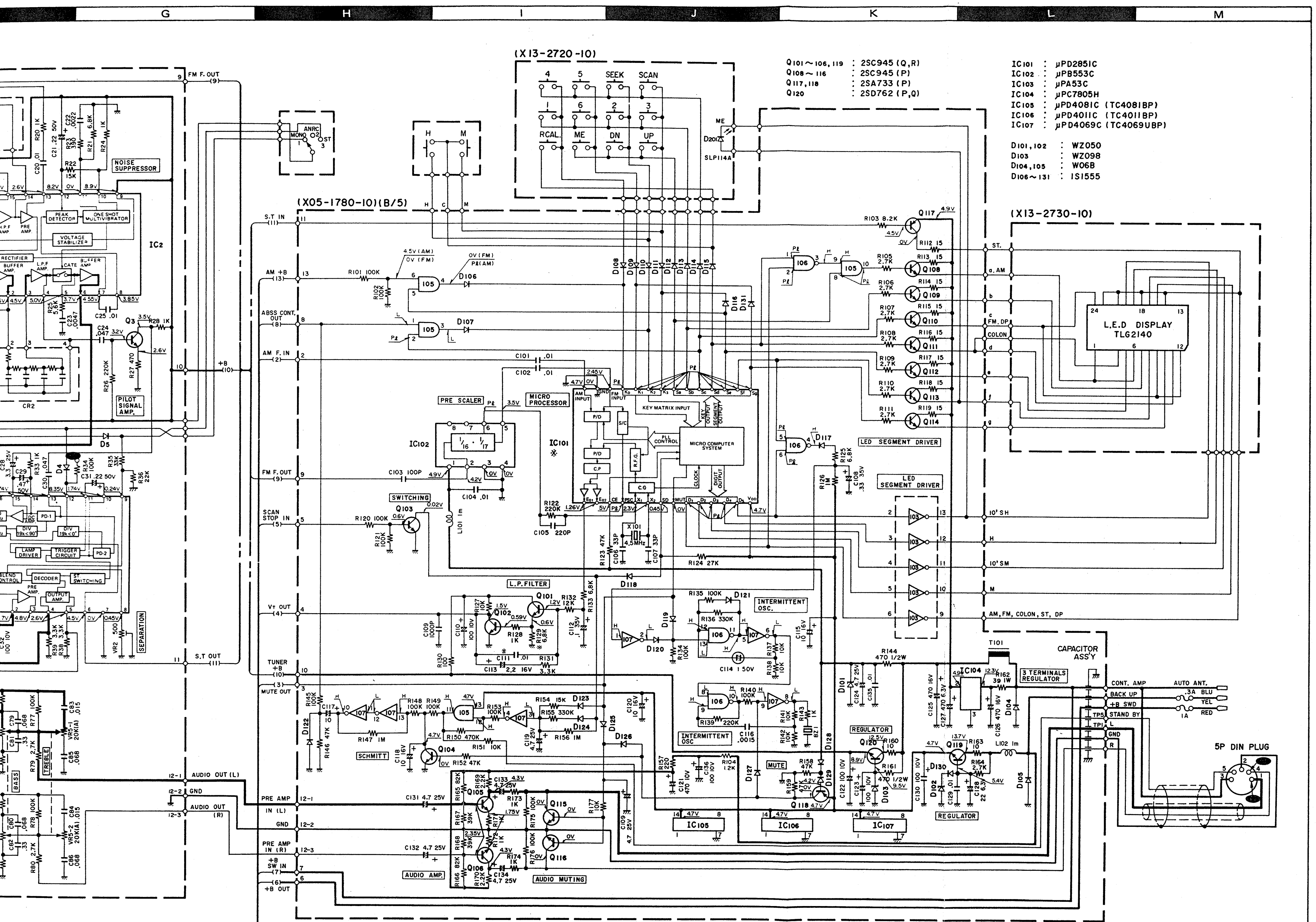
μPB533C

μPD2851C
μPD1702C-011

μPC7805H

2SK55

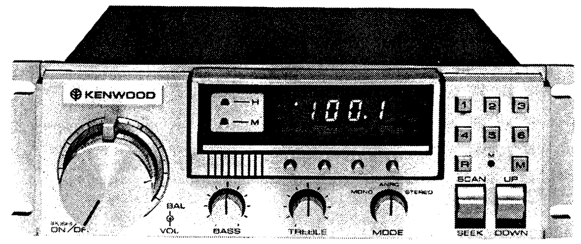
KTC-767



※ DESCRIPTION OF IC 101

IC 101	R129	C111	R122	C105	Pin NO. 6 of IC 102
μPD2851C	1K	.01	220K	220P	Connect to R122 & C105
μPD1702C-011	6.8K	.033			Connect to GND

NOTE. . H> 0.7 VDD , L < 0.3 VDD VDD ≒ 4.7
. Pℓ STANDS for PULSE LINE.
. DC VOLTAGES of Q101 & Q102 are at FM 87.9 MHz Condition (TENTATIVE).



SPECIFICATIONS

FM TUNER SECTION

Sensitivity (IHF)	1.1 μV (12 dBf)
50 dB Quieting Sensitivity	2.2 μV (13 dBf)
Frequency Response (−3 dB)	30 Hz to 15 kHz
Signal to Noise Ratio	73 dB (Mono)
Selectivity	80 dB
Stereo Separation	40 dB at 1 kHz
Capture Ratio	1.5 dB

AM TUNER SECTION

Sensitivity	30 μV
Selectivity	45 dB

PRE AMPLIFIER SECTION

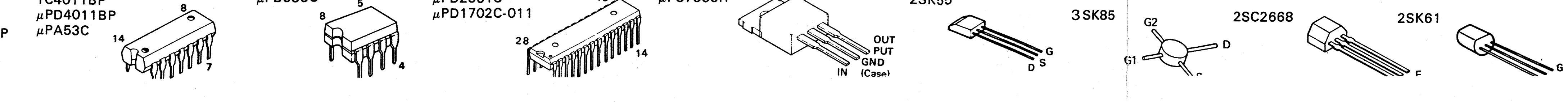
Bass	100 Hz ± 10 dB
Treble	10 kHz ± 10 dB
Max.Output Level/Impedance	300 mV/3 kohms
Operating Voltage	13.8V
Dimensions (W x H x D)	170 x 54 x 165 mm (6-11/16" x 2-1/8" x 6-1/2")
Body Size (W x H x D)	150 x 50 x 150 mm (5-15/16" x 2" x 5-15/16")
Weight	1.2 kg (2.6 lbs)

Kenwood follows a policy of continuous advancements in development. For this reason specifications may be changed without notice.

Kenwood strebt ständige Verbesserungen in der Entwicklung an. Daher bleiben Änderungen der technischen Daten jederzeit vorbehalten.

Kenwood poursuit une politique de progrès constants en ce qui concerne le développement. Pour cette raison, les spécifications sont sujettes à modifications sans préavis.

DC voltages are measured by a VOM with 20kΩ/V input impedance.



PARTS LIST

Ref. No. 参照番号	Parts No. 部品番号	Description 部品名／規格	Re-marks 備考
②			
① 18 1A	A01-0608-12	METALLIC CABINET	* ③
19 2A	A20-1979-11	FRONT PANEL ASSY	*K ④
19 2A	A20-1979-11	FRONT PANEL ASSY	PM
19 2A	A20-1979-11	FRONT PANEL ASSY	SU
19 2A	A20-1979-11	FRONT PANEL ASSY	XW
⑤ R221	R43-1333-15	FL-PROOF RD330 J 2H	* ⑥
R222	R43-1368-15	FL-PROOF RD680 J 2H	*
VR1 ,2	R12-3301-05	TRIMMING POT, 20K(B)	
VR3 ,4	R19-4305-05	POTENTIOMETER (OUTPUT)	*
VR5 ,6	R12-2302-05	TRIMMING POT, 5K(B)	

① Exploded view drawing No.
② Position in exploded view.
③ Symbol of new parts.
④ Area to which parts are shipped. Example: A20-1979-11 is the parts No. of FRONT PANEL ASS'Y for the "K" type products (for USA).
When this column is blank, it means that the same type of parts (same parts No.) are used for the products shipped to all areas.
⑤ Reference No. in schematic diagram.
⑥ Abbreviation of "Flame proof metal oxide film resistor". All capacitors and resistors are listed using abbreviations.
⑦ Abbreviations

* Abbreviations of capacitors (Parts No. with initial letter "C").

ELECTRO	Electrolytic capacitor
LL-ELEC	Low leak electrolytic capacitor
NP-ELEC	Non-pole electrolytic capacitor
MICA	Mica capacitor
POLYSTY	Polystyrene capacitor
MYLAR	Mylar capacitor
CERAMIC	Ceramic capacitor
TANTAL	Tantalum capacitor
MF	Metallized film capacitor
OIL	Oil capacitor

The unit "UF" is used in lieu of "μF".

* Abbreviations of resistors (Parts No. with initial letters "R").

RC	Carbon composition resistor	
RD	Carbon film resistor	
FL-PROOF RD	Flame-proof carbon film resistor	
RW	Wire wound power resistor	
FL-PROOF RS	Flame-proof metal oxide film resistor	
RN	Metal film resistor	
2B	Rated wattage	1/8W
2E	Rated wattage	1/4W
2H	Rated wattage	1/2W
3A	Rated wattage	1W
3D	Rated wattage	2W
3F	Rated wattage	3W
3G	Rated wattage	4W
3H	Rated wattage	5W

All resistor values are indicated with the unit (Ω) omitted

* Abbreviations common to capacitors and resistors.

C	±0.25pF (Used for capacitors only)
D	±0.5pF (Used for capacitors only)
F	±1%
G	±2%
J	±5%
K	±10%
M	±20%
Z	+80%, −20% (Used for capacitors only)
P	+100%, −0% (Used for capacitors only)

⑧ Resistors RD (carbon composition resistors) are not listed in the parts list. For values, refer to the schematic diagram.

Ref. No. 参照番号	Parts No. 部品番号	Description 部品名／規格	Re-marks 備考
KTC-767			
1 3A	- -	SHAFT	
2 2B	-	SUB CHASSIS	
3 2B	-	SUB PANEL	
4 3B	-	BOTTOM PLATE	
5 2A	-	BADGE	
6 3B	-	LEVER,ARM	
7 3A	-	RETAINER	
8 1B	-	HOLDER	
9 3A	-	SHADE	
10 1A	A01-0370-03	METALLIC CABINET	*
11 2A	A20-1595-03	FRONT PANEL ASSY	*
12 2A	B01-0161-02	PANEL ESCUTCHEON	*
13 1A	B01-0162-03	PANEL ESCUTCHEON	*
14 3A	B01-0165-03	PANEL ESCUTCHEON ASSY	*
15 3A	B03-0146-04	DRESSING PLATE	*
16 3A	B08-8001-04	INDICATOR WINDOW	*
17 2A	B19-0218-03	LIGHTING RING	
-	B46-0063-13	WARRANTY CARD	U
-	B46-0070-03	WARRANTY CARD	KU
-	B46-0071-03	WARRANTY CARD	P
-	B50-3109-00	INSTRUCTION MANUAL	*K
-	B50-3109-00	INSTRUCTION MANUAL	*U
-	B50-3110-00	INSTRUCTION MANUAL	*P
18 1B	E30-0627-05	DC CORD (YEL)	*
19 1B	E30-0628-05	DC CORD (RED)	*
20 1B	E30-0629-05	DC CORD (GRN)	*
21 1B	E30-0631-05	DIN CORD	*
22 1B	E30-0632-05	ANT CORD	*
-	E30-0630-05	EARTH CORD (BLK)	*
23 2B	F20-0144-04	INSULATOR	*
24 2A	G10-0030-04	SHEET	*
-	H01-3124-04	CARTON BOX	*K
-	H01-3125-04	CARTON BOX	*P
-	H10-1545-03	POLYSTYRENE FIXTURE	
-	H25-0067-03	BAG	
-	H25-0112-04	BAG	
-	H25-0162-04	BAG	
25 2B	J02-0108-04	FOOT	
26 2A	K23-0336-04	KNOB	*
27 2A	K23-0337-04	KNOB	*
28 3A	K27-0122-04	KNOB	*
29 2B	K27-0123-04	KNOB	*
30 2B	K27-0124-04	KNOB ASSY	*
31 2A	K29-0335-04	KNOB	*
-	N99-0023-05	SCREW NUT SET	
32 1A3B	X05-1780-10	TUNER PCB ASSY	*
33 2B	X13-2720-10	SW PCB ASSY	*
34 1A	X13-2730-10	SUB PCB ASSY	*
TUNER(X05-1780-10)			
35 2B	B30-0217-05	LAMP	*
36 1A	C91-0113-05	CAPACITOR ASSY	*
C1 -5	C55-1710-38	CERAMIC 0.01UF Z	
C6 ,7	C24-1710-59	ELECTRO 1UF 50WV	
C8	C55-1747-38	CERAMIC 0.047UF Z	

PARTS LIST

Ref. No. 参照番号	Parts No. 部品番号	Description 部品名／規格	Re-marks 備考
C9	C71-1722-15	CERAMIC 220PF J	
C10 ,11	C55-1747-38	CERAMIC 0.047UF Z	
C12 ,13	C55-1710-38	CERAMIC 0.01UF Z	
C14	C24-1410-69	ELECTRO 10UF 25WV	
C15	C24-1722-49	ELECTRO 0.22UF 50WV	
C16	C71-1722-15	CERAMIC 220PF J	
C17	C24-1710-59	ELECTRO 1UF 50WV	
C18	C71-1733-16	CERAMIC 330PF J	
C19	C71-1705-01	CERAMIC 5PF C	
C20	C91-0117-05	CERAMIC 0.01UF K	*
C21	C25-1722-47	LL-ELEC 0.22UF 50WV	
C22	C91-0116-05	CERAMIC 0.0022UF K	*
C23	C91-0105-05	CERAMIC 0.0047UF K	
C24	C91-0119-05	CERAMIC 0.047UF K	*
C25	C91-0117-05	CERAMIC 0.01UF K	*
C26	C50-2051-15	MP 510PF J	
C27	C24-1710-59	ELECTRO 1UF 50WV	
C28	C25-1433-57	LL-ELEC 3.3UF 25WV	
C29	C25-1747-47	LL-ELEC 0.47UF 50WV	
C30	C91-0119-05	CERAMIC 0.047UF K	*
C31	C25-1722-47	LL-ELEC 0.22UF 50WV	
C32	C24-1010-79	ELECTRO 100UF 10WV	
C33 ,34	C45-1727-25	MYLAR 0.0027UF J	
C35 ,36	C24-1710-59	ELECTRO 1UF 50WV	
C37	C52-1710-26	CERAMIC 0.001UF K	
C38	C24-1710-59	ELECTRO 1UF 50WV	
C39	C24-1710-59	CERAMIC 0.001UF K	
C40	C71-1710-15	CERAMIC 100PF J	
C41	C50-2039-15	MP 390PF J	
C42	C71-1710-02	CERAMIC 10PF D	
C43	C24-1010-79	ELECTRO 100UF 10WV	
C44	C71-1710-15	CERAMIC 100PF J	
C45	C91-0117-05	CERAMIC 0.01UF K	
C46 ,47	C55-1747-38	CERAMIC 0.047UF Z	
C48	C24-1410-69	ELECTRO 10UF 25WV	
C49	C55-1710-38	CERAMIC 0.01UF Z	
C50 ,51	C55-1747-38	CERAMIC 0.047UF Z	
C52 -54	C55-1710-38	CERAMIC 0.01UF Z	
C55	C24-1410-69	ELECTRO 10UF 25WV	
C56	C55-1747-38	CERAMIC 0.047UF Z	
C57	C91-0117-05	CERAMIC 0.01UF K	*
C58	C55-1710-38	CERAMIC 0.01UF Z	
C59	C91-0117-05	CERAMIC 0.01UF K	*
C60	C24-1222-69	ELECTRO 22UF 16WV	
C61	C24-1410-69	ELECTRO 10UF 25WV	
C62	C26-1722-57	NP-ELEC 2.2UF 50WV	
C63	C26-1747-47	NP-ELEC 0.47UF 50WV	
C64	C24-1722-49	ELECTRO 0.22UF 50WV	
C65	C71-1747-05	CERAMIC 47PF J	
C66 -69	C55-1710-38	CERAMIC 0.01UF Z	
C70 ,71	C91-0105-05	CERAMIC 0.0047UF K	
C72 ,73	C91-0121-05	CERAMIC 0.1UF M	*
C74	C24-1047-69	ELECTRO 47UF 10WV	
C75 ,76	C24-1710-59	ELECTRO 1UF 50WV	
C79 ,80	C91-0120-05	CERAMIC 0.068UF K	*
C81 ,82	C91-0114-05	MYLAR 0.33UF J	*
C83 ,84	C91-0118-05	CERAMIC 0.015UF K	*
C85 ,86	C91-0120-05	CERAMIC 0.068UF K	*
C101,102	C55-1710-38	CERAMIC 0.01UF Z	
C103	C71-1710-15	CERAMIC 100PF J	
C104	C55-1710-38	CERAMIC 0.01UF Z	
C105	C71-1722-15	CERAMIC 220PF J	

Ref. No. 参照番号	Parts No. 部品番号	Description 部品名／規格	Re-marks 備考
C106,107	C63-1733-05	CERAMIC 33PF J	
C108	C25-1733-47	LL-ELEC 0.33UF 50WV	
C109	C24-1747-59	ELECTRO 4.7UF 50WV	
C110	C24-1010-79	ELECTRO 100UF 10WV	
C111	C45-1733-35	MYLAR 0.033UF J	
C112	C25-1710-47	LL-ELEC 0.1UF 50WV	
C113	C25-1422-57	LL-ELEC 2.2UF 25WV	
C114	C26-1710-57	NP-ELEC 1UF 50WV	
C115	C24-1410-69	ELECTRO 10UF 25WV	
C116	C91-0115-05	CERAMIC 0.0015UF K	*
C117	C24-1410-69	ELECTRO 10UF 25WV	
C118	C25-1410-67	LL-ELEC 10UF 25WV	
C119	C25-1447-57	LL-ELEC 4.7UF 25WV	
C120	C24-1410-69	ELECTRO 10UF 25WV	
C121	C24-1047-79	ELECTRO 100UF 10WV	
C123	C24-1010-79	ELECTRO 100UF 10WV	
C124	C24-1747-59	ELECTRO 4.7UF 50WV	
C125,126	C90-0820-05	ELECTRO 470UF 16WV	
C127	C24-0847-79	ELECTRO 470UF 6.3WV	
C128	C24-1222-69	ELECTRO 22UF 16WV	
C129	C55-1710-38	CERAMIC 0.01UF Z	
C130	C24-1010-79	ELECTRO 100UF 10WV	
C131-134	C24-1747-59	ELECTRO 4.7UF 50WV	
C135	C55-1710-38	CERAMIC 0.01UF Z	
C136	C24-1010-79	ELECTRO 100UF 10WV	
TC1 ,2	C05-0303-05	TRIMMER CAPACITOR	
-	E10-0601-05	PC BOARD CONNECTOR	*
-	E10-0901-05	PC BOARD CONNECTOR	*
-	E31-1380-05	PARALLEL WIRE	*
-	E31-1381-05	PARALLEL WIRE	*
-	E40-0373-05	PIN CONNECTOR	
-	E40-0473-05	PIN CONNECTOR	
-	E40-0673-05	PIN CONNECTOR	
CF1 ,2	L72-0086-05	CERAMIC FILTER	*
CF3	L72-0082-05	CERAMIC FILTER	
L1	L40-4791-61	INDUCTOR 4.7UH K	
L2	L40-1092-44	INDUCTOR 1UH M	
L3	L40-2292-44	INDUCTOR 2.2UH M	
L4	L33-0281-05	CHOCK COIL	*
L5	L30-0347-05	IFT	*
L6	L30-0348-05	IFT	*
L7	L31-0452-05	RF COIL	*
L8	L32-0238-05	OSCILLATING COIL	*
L9	L31-0453-05	RF COIL	*
L10	L30-0337-05	IFT	
L11	L30-0349-05	IFT	
L12	L30-0283-05	IFT	
L101,102	L40-1021-45	INDUCTOR 1MH K	
T101	L15-0016-05	CHOKE COIL	*
X101	L77-0573-05	CRYSTAL RESONATOR	*
CR1	R90-0130-05	MULTIPLE COMPONENTS	*
CR2	R90-0129-05	MULTIPLE COMPONENTS	*
CR3 ,4	R90-0131-05	MULTIPLE COMPONENTS	*
R144	R40-8347-16	RC 470 K 2H	
R161	R40-8347-16	RC 470 K 2H	
R162	R47-5415-05	FL-PROOF RS15 J 3A	
VR1	R12-2302-05	POTENTIOMETER 5K	
VR2	R12-0302-05	POTENTIOMETER 500	
VR3	R24-9007-05	POTENTIOMETER 20K (B)	*
VR4 ,5	R10-3004-05	POTENTIOMETER 20K (A)	*

PARTS LIST

Ref. No. 参照番号	Parts No. 部品番号	Description 部品名／規格		Remarks 備考
C9	C71-1722-15	CERAMIC	220PF J	
C10 ,11	C55-1747-38	CERAMIC	0.047UF Z	
C12 ,13	C55-1710-38	CERAMIC	0.01UF Z	
C14	C24-1410-69	ELECTRO	10UF 25WV	
C15	C24-1722-49	ELECTRO	0.22UF 50WV	
C16	C71-1722-15	CERAMIC	220PF J	
C17	C24-1710-59	ELECTRO	1UF 50WV	
C18	C71-1733-16	CERAMIC	330PF J	
C19	C71-1705-01	CERAMIC	5PF C	
C20	C91-0117-05	CERAMIC	0.01UF K	*
C21	C25-1722-47	LL-ELEC	0.22UF 50WV	
C22	C91-0116-05	CERAMIC	0.0022UF K	*
C23	C91-0105-05	CERAMIC	0.0047UF K	
C24	C91-0119-05	CERAMIC	0.047UF K	*
C25	C91-0117-05	CERAMIC	0.01UF K	*
C26	C50-2051-15	MP	510PF J	
C27	C24-1710-59	ELECTRO	1UF 50WV	
C28	C25-1433-57	LL-ELEC	3.3UF 25WV	
C29	C25-1747-47	LL-ELEC	0.47UF 50WV	
C30	C91-0119-05	CERAMIC	0.047UF K	*
C31	C25-1722-47	LL-ELEC	0.22UF 50WV	
C32	C24-1010-79	ELECTRO	100UF 10WV	
C33 ,34	C45-1727-25	MYLAR	0.0027UF J	
C35 ,36	C24-1710-59	ELECTRO	1UF 50WV	
C37	C52-1710-26	CERAMIC	0.001UF K	
C38	C24-1710-59	ELECTRO	1UF 50WV	
C39	C24-1710-59	CERAMIC	0.001UF K	
C40	C71-1710-15	CERAMIC	100PF J	
C41	C50-2039-15	MP	390PF J	
C42	C71-1710-02	CERAMIC	10PF D	
C43	C24-1010-79	ELECTRO	100UF 10WV	
C44	C71-1710-15	CERAMIC	100PF J	
C45	C91-0117-05	CERAMIC	0.01UF K	
C46 ,47	C55-1747-38	CERAMIC	0.047UF Z	
C48	C24-1410-69	ELECTRO	10UF 25WV	
C49	C55-1710-38	CERAMIC	0.01UF Z	
C50 ,51	C55-1747-38	CERAMIC	0.047UF Z	
C52 -54	C55-1710-38	CERAMIC	0.01UF Z	
C55	C24-1410-69	ELECTRO	10UF 25WV	
C56	C55-1747-38	CERAMIC	0.047UF Z	
C57	C91-0117-05	CERAMIC	0.01UF K	*
C58	C55-1710-38	CERAMIC	0.01UF Z	
C59	C91-0117-05	CERAMIC	0.01UF K	*
C60	C24-1222-69	ELECTRO	22UF 16WV	
C61	C24-1410-69	ELECTRO	10UF 25WV	
C62	C26-1722-57	NP-ELEC	2.2UF 50WV	
C63	C26-1747-47	NP-ELEC	0.47UF 50WV	
C64	C24-1722-49	ELECTRO	0.22UF 50WV	
C65	C71-1747-05	CERAMIC	47PF J	
C66 -69	C55-1710-38	CERAMIC	0.01UF Z	
C70 ,71	C91-0105-05	CERAMIC	0.0047UF K	
C72 ,73	C91-0121-05	CERAMIC	0.1UF M	*
C74	C24-1047-69	ELECTRO	47UF 10WV	
C75 ,76	C24-1710-59	ELECTRO	1UF 50WV	
C79 ,80	C91-0120-05	CERAMIC	0.068UF K	*
C81 ,82	C91-0114-05	MYLAR	0.33UF J	*
C83 ,84	C91-0118-05	CERAMIC	0.015UF K	*
C85 ,86	C91-0120-05	CERAMIC	0.068UF K	*
C101,102	C55-1710-38	CERAMIC	0.01UF Z	
C103	C71-1710-15	CERAMIC	100PF J	
C104	C55-1710-38	CERAMIC	0.01UF Z	
C105	C71-1722-15	CERAMIC	220PF J	

Ref. No. 参照番号	Parts No. 部品番号	Description 部品名／規格		Remarks 備考
C106,107	C63-1733-05	CERAMIC	33PF J	
C108	C25-1733-47	LL-ELEC	0.33UF 50WV	
C109	C24-1747-59	ELECTRO	4.7UF 50WV	
C110	C24-1010-79	ELECTRO	100UF 10WV	
C111	C45-1733-35	MYLAR	0.033UF J	
C112	C25-1710-47	LL-ELEC	0.1UF 50WV	
C113	C25-1422-57	LL-ELEC	2.2UF 25WV	
C114	C26-1710-57	NP-ELEC	1UF 50WV	
C115	C24-1410-69	ELECTRO	10UF 25WV	
C116	C91-0115-05	CERAMIC	0.0015UF K	*
C117	C24-1410-69	ELECTRO	10UF 25WV	
C118	C25-1410-67	LL-ELEC	10UF 25WV	
C119	C25-1447-57	LL-ELEC	4.7UF 25WV	
C120	C24-1410-69	ELECTRO	10UF 25WV	
C121	C24-1047-79	ELECTRO	100UF 10WV	
C123	C24-1010-79	ELECTRO	100UF 10WV	
C124	C24-1747-59	ELECTRO	4.7UF 50WV	
C125,126	C90-0820-05	ELECTRO	470UF 16WV	
C127	C24-0847-79	ELECTRO	470UF 6.3WV	
C128	C24-1222-69	ELECTRO	22UF 16WV	
C129	C55-1710-38	CERAMIC	0.01UF Z	
C130	C24-1010-79	ELECTRO	100UF 10WV	
C131-134	C24-1747-59	ELECTRO	4.7UF 50WV	
C135	C55-1710-38	CERAMIC	0.01UF Z	
C136	C24-1010-79	ELECTRO	100UF 10WV	
TC1 ,2	C05-0303-05	TRIMMER CAPACITOR		
-	E10-0601-05	PC BOARD CONNECTOR		*
-	E10-0901-05	PC BOARD CONNECTOR		*
-	E31-1380-05	PARALLEL WIRE		*
-	E31-1381-05	PARALLEL WIRE		*
-	E40-0373-05	PIN CONNECTOR		
-	E40-0473-05	PIN CONNECTOR		
-	E40-0673-05	PIN CONNECTOR		
CF1 ,2	L72-0086-05	CERAMIC FILTER		*
CF3	L72-0082-05	CERAMIC FILTER		
L1	L40-4791-61	INDUCTOR	4.7UH K	
L2	L40-1092-44	INDUCTOR	1UH M	
L3	L40-2292-44	INDUCTOR	2.2UH M	
L4	L33-0281-05	CHOCK COIL		*
L5	L30-0347-05	IFT		*
L6	L30-0348-05	IFT		*
L7	L31-0452-05	RF COIL		*
L8	L32-0238-05	OSCILLATING COIL		*
L9	L31-0453-05	RF COIL		*
L10	L30-0337-05	IFT		
L11	L30-0349-05	IFT		
L12	L30-0283-05	IFT		
L101,102	L40-1021-45	INDUCTOR	1MH K	
T101	L15-0016-05	CHOKE COIL		*
X101	L77-0573-05	CRYSTAL RESONATOR		*
CR1	R90-0130-05	MULTIPLE COMPONENTS		*
CR2	R90-0129-05	MULTIPLE COMPONENTS		*
CR3 ,4	R90-0131-05	MULTIPLE COMPONENTS		*
R144	R40-8347-16	RC	470 K 2H	
R161	R40-8347-16	RC	470 K 2H	
R162	R47-5415-05	FL-PROOF RS	15 J 3A	
VR1	R12-2302-05	POTENTIOMETER	5K	
VR2	R12-0302-05	POTENTIOMETER	500	
VR3	R24-9007-05	POTENTIOMETER	20K (B)	*
VR4 ,5	R10-3004-05	POTENTIOMETER	20K (A)	*

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PARTS LIST

Ref. No. 参照番号	Parts No. 部品番号	Description 部品名／規格	Remarks 備考
S1	S40-4030-15	PUSH SWITCH	*
S2 -4	S40-2107-05	PUSH SWITCH	*
S5	S29-2022-05	ROTARY WAFER SWITCH	*
BZ1	T95-0004-05	CERAMIC BUZZER FIG101	*
D1 -5	V11-0076-05	1S1555	
D6 -8	V11-6100-60	SVC321-3(A,B)	*
D9	V11-0051-05	1N60	
D101,102	V11-4102-10	WZ-050	
D103	V11-4107-10	WZ-098	
D104,105	V11-0295-05	W06B	
D106-130	V11-0076-05	1S1555	
IC1	V30-0438-10	HA12411	*
IC2	V30-0440-10	HA11219	*
IC3	V30-0441-10	KB4448	*
IC4	V30-0439-10	LA1130	*
IC5	V30-0442-10	AN7311	*
IC107	V30-0297-20	TC4069UBP UPD4069C	
IC106	V30-0301-70	TC4011BP UPD4011BP	
IC105	V30-0399-10	UPD4081C TC4081BP	
Q5	V03-1675-00	2SC1675	
IC102	V30-0443-10	UPB553C	*
IC101	V30-0444-10	UPD2851C,UPD1702C-011	*
IC103	V30-0445-10	UPA53C	*
IC104	V30-0446-10	UPC7805H	*
Q1	V03-1923-00	2SC1923	*
Q2～4,6,8	V03-0270-05	2SC945(R,Q)	
Q7	V09-0151-10	2SK193(K,L)	*
Q10 -11	V03-0270-05	2SC945(R,Q)	
Q9	V03-1923-00	2SC1923	*
Q101-106	V03-0270-05	2SC945(R,Q)	
Q108-116	V03-0405-05	2SC945(P)	
Q117,118	V01-0733-11	2SA733(A)(P)	
Q119	V03-0270-05	2SC945(R,Q)	
Q120	V04-0762-10	2SD762(Q,P)	
-	W02-0031-05	FM FRONT END FIG102	*
Frontend (W02-0031-05)			
Q1	V09-0150-10	3SK85	
Q2	V03-2668-16	2SC2668	
Q3	V09-0121-10	2SK55	
Q4	V09-0124-20	2SK61	
D1～4	V11-2103-50	1SV55	*
SW(X13-2720-10)			
D201	B30-0221-05	SLP114A (LAMP)	
-	S40-1016-05	PUSH SWITCH	*
-	S40-1017-05	PUSH SWITCH	*
-	S40-1018-05	PUSH SWITCH	*
SUB(X13-2730-10)			
-	B30-0220-05	PR2434D (LAMP)	*
-	B38-0011-05	DISPLAY ASSY	*
-	E31-1385-05	PARALLEL WIRE	*
-	J25-1734-04	PARALLEL WIRE	*

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KENWOOD®
STEREO FOR YOUR CAR

SERVICE MANUAL

KTC-767

SUPPLEMENT

CIRCUIT DESCRIPTION

Operation of PLL Circuit

A basic PLL circuitry is shown in Fig. 1

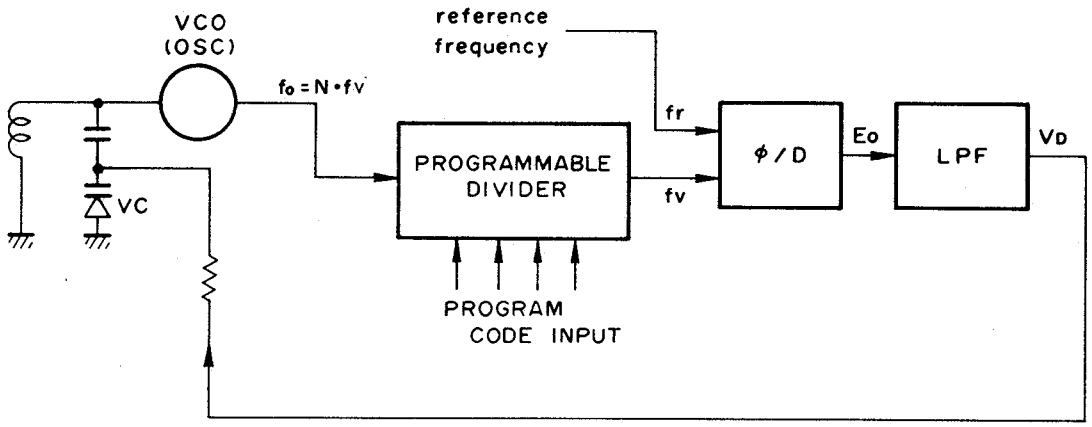


Fig. 1

In the above figure, VCO is a voltage controlled oscillator, the frequency of which is varied with the capacitance change of VC (variable capacitance diode or varactor-diode) due to the application of DC reverse bias voltage V_D. When the VCO frequency fo is applied to the programmable divider ($\div$N), the frequency is divided by N and the output frequency of fv = fo/N is made and led into the ϕ/D (Phase Detector). Both the reference frequency (fr) and fv are compared with each other at ϕ/D and if there is a frequency or phase difference, the ϕ/D produces the error output (Eo) proportional to the difference.

Since the Eo is of pulse shape, this is led to the Low Pass Filter (LPF) and converted into smooth DC voltage. The DC voltage is then applied to VC. In considering the chains between fo and V_D, if fv coincides with fr, namely Eo = 0, the following equation will be established.

$$fr = fv = \frac{fo}{N} \qquad fo = N \cdot fr$$

Where, N is a programmable number (code) consisting of a combination of "0" and "1". If "N" is varied, the fo will vary with N. Therefore, if the VCO is used as a local oscillator in a receiver circuit, the received frequency can be varied by varying the number of "N".

Generally, fr is selected equal to the channel spacing of the broadcast stations. Therefore, if the receive band is decided, fo and fr will be fixed accordingly. Then, the value of N is also decided.

Since the frequency stability of fo is markedly depends upon that of the reference frequency fr, a crystal oscillator is generally used as the reference oscillator.

PLL Receiver

The basic configuration of digital-controlled tuning system employing PLL is given in Figure 2.

Since the V_D is used as a bias voltage to the varicap diode VC for RF tuned circuit, both varicap diodes (one for RF and another for VCO circuits) should be operated to meet their tracking condition precisely.

CIRCUIT DESCRIPTION

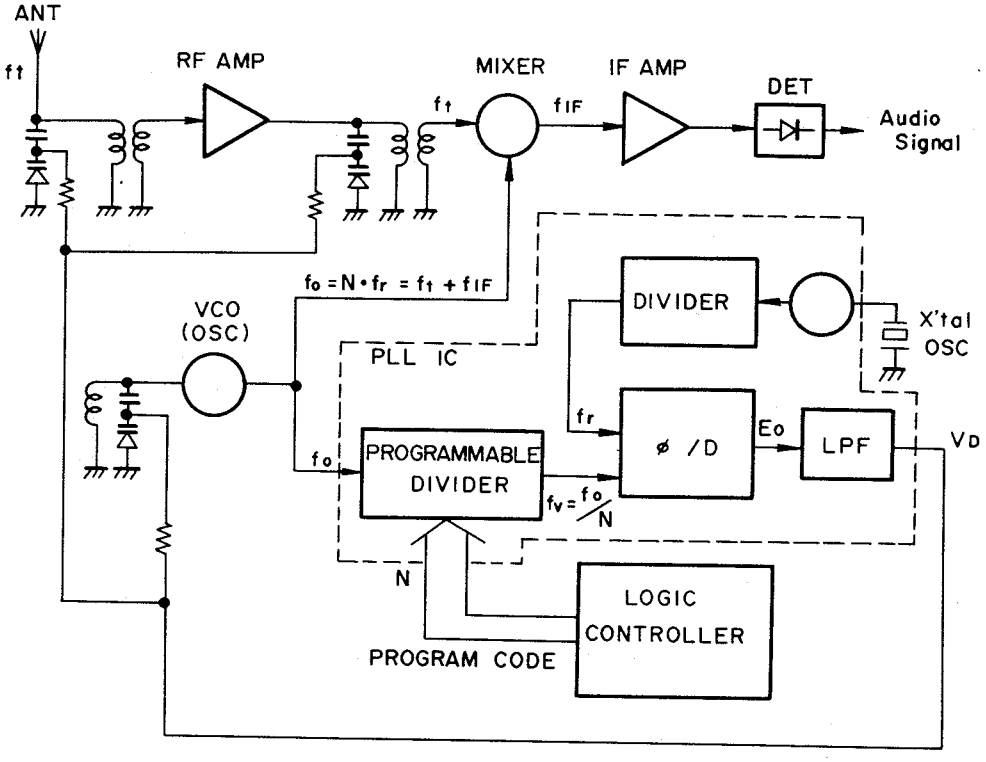


Fig. 2

The μPD2851/μPD1702C-011 4-bit CMOS Micro-controller for Digital Tuning (Port Cofiguration)

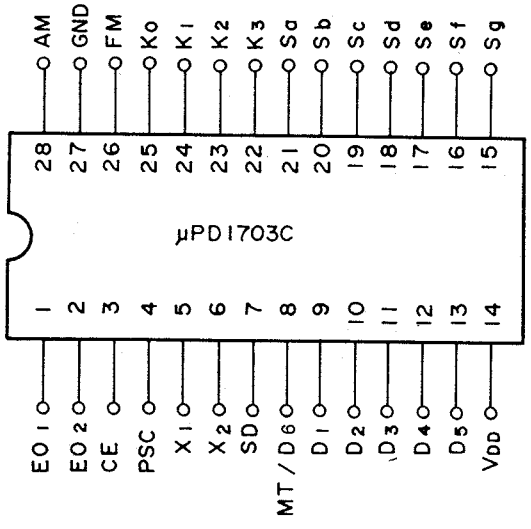


Fig. 3

NOTE:
This integrated circuit is a micro-controller specially designed for electronic tuners, incorporating a PLL digital synthesizer and a 4-bit microcomputer, and it has the system numbers μPD1701C and μPD1703C. When the system program is stored in the device, it has numbers such as μPD2851C.

Port Names and Functions

1. E01, E02 (Error Out): Port No. 1, 2

These are the PLL error output lines.

This output goes high when the oscillation frequency divided by a value which is set in the programmable divider is higher than the reference frequency, goes low when the former is lower than the latter, and has high impedance when both are equal.

Usually, these lines are connected to the inverted input of the filter amplifier for the low pass filter (LPF), the output of which is the VCO control voltage. In this model pin E01 is used for both AM and FM reception.

2. CE (Chip Enable): Port No. 3

This input port is for the IC device selection signal. The IC device is activated when a high level is applied; this line is kept low when it is not operated and the power is only supplied to the memory. In this model, this line is fixed at high level, so that it goes low only when the power is turned off.

3. MT/D6 (Muting/Digit Output): Port No. 8

The output signal on this line prevents noise when the PLL goes out of phase by a tuning operation, and it is controlled by the DIG command. The line goes high during a tuning operation, so that audio muting is carried out to reduce noise.

CIRCUIT DESCRIPTION

4. PSC (Prescaler Control): Port No. 4

This line outputs the selection signal of the dividing ratio to the two-modulus Prescaler (μPB553C) when the Pulse Swallow system is used for the divider. This pulse signal is generated at each rising edge of the FM signal applied to pin 26, until the Swallow Counter goes to a 0. During this period, the dividing ratio is 1/17. When the Swallow Counter gets to a 0, this output goes low and the dividing ratio becomes 1/16. The μPD2851C employs the Pulse Swallow system, and μPD1702C-011 employs the 1/16-fixed dividing system.

5. X1, X2 (Crystal): Port No. 5, 6

A 4.5 MHz crystal is connected to these lines.

6. SD (Station Detector): Port No. 7

This is the 1-bit input port for detecting the reception of a broadcast. In the μPD2851C and μPD1702C-011, scanning is stopped by the program when a high level signal is applied to this line during automatic tuning.

7. D1-D5 (Digit Outputs): Port No. 9~13

These lines send out the digital display signals.

The contents of registers in data memory (RAM) are loaded into the digit Programmable Logic Array (PLA), and output on these lines. In the μPD2851C and μPD1702-011, D1 indicates a dot symbol and D2 through D5 indicate numerals giving the time and frequency.

8. V_{DD} (+5V ±10%): Port No. 14

This is the power line of this IC.

A voltage of +5V ±10% must be supplied when the device is operating, and the voltage can be reduced to +3.5V, which is supplied to the internal data memory (RAM), when the device is not operating. The CPU starts operation at least 50 ms after the power has been supplied, when the crystal oscillator has stabilized. When the power is switched on, the timer flip-flop is reset so that the program is started from address 00. (Power-ON reset system)

9. AM (Direct System Oscillator Input): Port No. 28

This input port is for the VCO oscillation signal when the two-modulus Prescaler is not used, but the CPU specifies the Direct system (band L) instead of the internal PLL system. The Direct system is specified when the VCO frequency is lower than 2.5 MHz.

In use as an AM tuner, the local oscillator output is supplied on this line.

10. FM (Pulse Swallow System Oscillator Input): Port No. 26

This input port is for the VCO oscillation signal when the CPU specifies the Pulse Swallow system (band H) using the two-modulus Prescaler (μPB553C) with the dividing ratio of 1/16 and 1/17, at the internal PLL system.

When the device is used in an FM tuner, the local oscillator frequency divided by 1/16 and 1/17 using the μPB553C (Two-modulus Prescaler) is supplied. In the μPD1702C-011, this line is used as the input port for the Direct (fixed-divider) system.

11. K0~K3 (Key Return Signal Inputs): Port No. 22 ~ 25

These input ports are for the key return signals from the external key matrix.

12. Sa~Sg (Segment Outputs): Port No. 15~21

These lines send out the segment signals for display. The contents of registers in data memory (RAM) are loaded in the segment PLA (Programmable Logic Array) by the SEG command, and sent out on these lines. These outputs are also used as the key return signals for the key matrix.

Internal System Structure

The μPD1701C and μPD1703C have the system structure as shown in the figure on the next page, and it can be divided into the PLL section and CPU section.

CIRCUIT DESCRIPTION

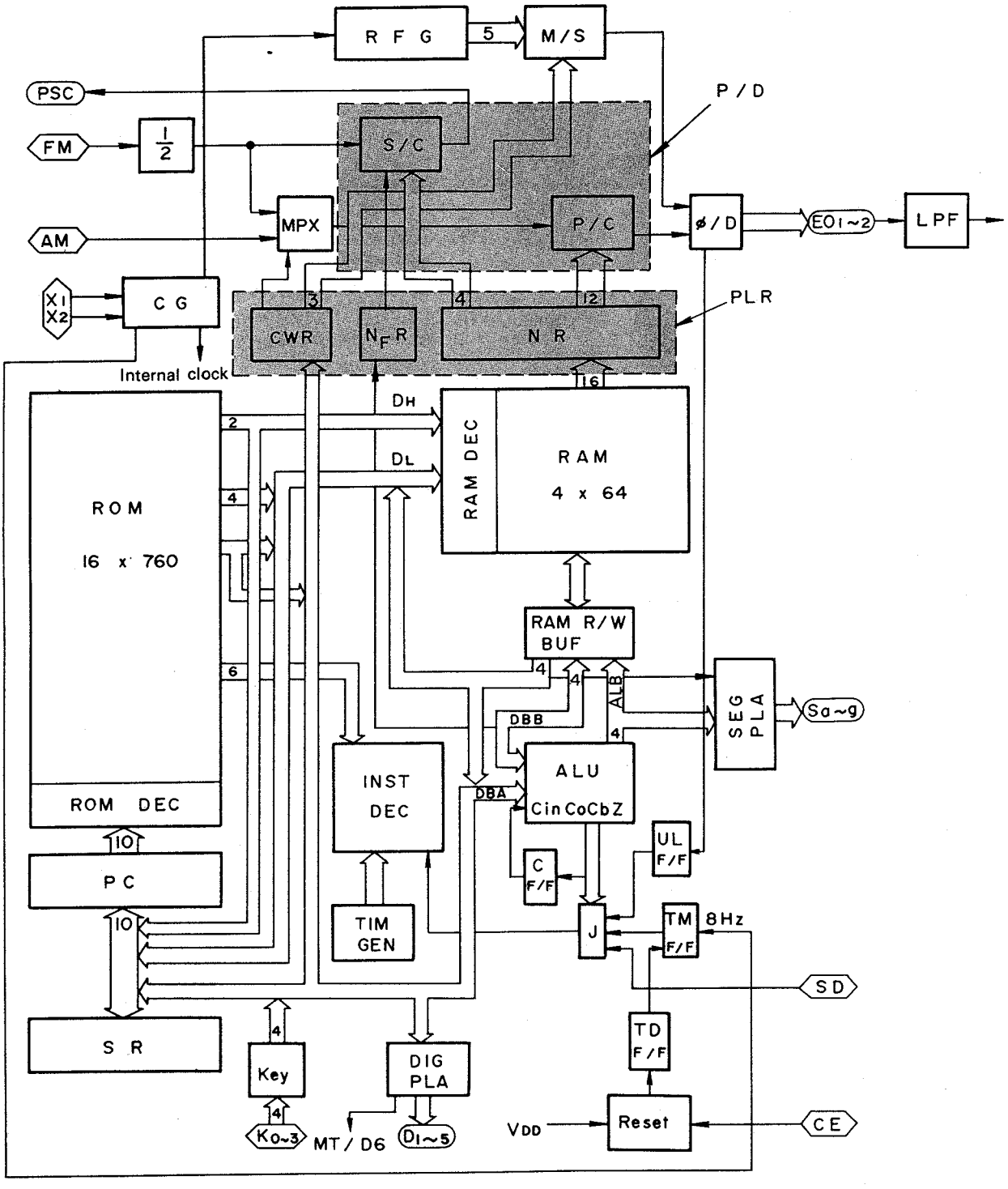


Fig. 4

CIRCUIT DESCRIPTION

1. PLL section

This section includes a reference frequency generator (RFG), mode selector (M/S), phase detector (ϕ/D), programmable divider (P/D), and PLL register (PLR).

1) Reference frequency generator (RFG)

The RFG produces reference frequencies to be compared with a VCO frequency which is divided by the programmable divider (P/D). The RFG receives a 450 kHz clock from the clock generator in the CPU section, and divides the frequency to form the five reference frequencies (fr) 1 kHz, 5 kHz, 9 kHz, 10 kHz, and 25 kHz. One of these reference frequencies is selected by the program to best meet the reception band and region.

In the United Sates, the reference frequency is 10 kHz for AM reception and 25 kHz for FM reception. However, because of the limited quality of components, the reference frequency often appears in the audible band such as at 5 kHz and 6.25 kHz, causing beats. The μPD2851C employs the Pulse Swallow system which makes it possible for the reference frequency of 25 kHz to be selected, so that beats are prevented.

2) Phase detector (ϕ/D)

This circuit detects the phase difference between the reference frequency signal (fr) and the VCO output whose frequency is divided by the programmable divider (P/D).

When the frequency-divided VCO output (fosc/N is higher than fr, the ϕ/D circuit produces a signal named High till both frequencies fosc/N and fr matches. When the fosc/N is lower than fr, the ϕ/D circuit produces Low signal till fosc/N and fr matches. When they match, it becomes high-impedance.These outputs are stored in the internal charge pump, resulting in the following state of pins E01 and E02.

1. fr $>$ fosc/N ..... Low
2. fr $<$ fosc/N ..... High
3. fr $=$ fosc/N ..... High impedance

Where N is the dividing ratio, fosc is the frequency of VCO.

This output is fed back to the VCO via the low pass filter.

3) Programmable divider (P/D)

The programmable divider consists of a Swallow Counter (S/C) and a programmable counter (P/C). The Swallow Counter is a 5-bit presettable down counter in which the contents of the NR0 of the N register (NR) and the contents of the N_F register (N_FR) are preset. The N_FR's contents are preset to the least significant bit of the S/C. The S/C is decremented by the output of the μPB553 two-modulus Prescaler, the frequency of which is halved. When the output of S/C becomes all zero, it is indicated to the prescaler via the PSC line (pin 4) to specify the 1/16 dividing mode. The P/C is a 12-bit frequency divider which is presettable with the contents of NR1-NR3 as the divisor (the second and higher significant bits of the divider), and it is decremented simultaneously with the S/C.

4) PLL register (PLR)

The following information is necessary to control the PLL.

1. Reference frequency (f_r)
2. Frequency dividing system
3. Dividing ratio (N)

The PLL register (PLR) corresponds to a specific address in data memory (RAM) where the above information is stored, and it is transferred to the PLR by a PLL command. The PLR consists of four 4-bit registers (NR0-NR3) which are called "N register (NR)", a 1-bit NF register (NFR), and a 4-bit control word register (CWR).

The control word desginates the reference frequency and the frequency division system. There are two frequency dividing systems: the Direct system which is specified when the input frequency of the PLL section is lower than 2.5 MHz (band L) and the Pulse Swallow system which is specified when the frequency is higher than 2.5 MHz and lower than 8.8 MHz (band H).

2. CPU section

This section includes a clock generator (CG), program counter (PC), stack register (SR), program memory (ROM), general-purpose register (GR), data memory (RAM), arithmetic logic unit (ALU), timer flip-flop (TM F/F), timer disable flip-flop (TD F/F), unlock flip-flop (UL F/F), carry flip-flop (C F/F), judge (J), key, segment programmable logic array (SEG PLA), digit programmable logic array (DIG PLA), and reset circuit.

1) Clock generator (CG)

The CG generates various frequencies which are necessary for the CPU operation and the reference frequency in the PLL section as well as controlling timer operation. A 4.5 MHz crystal is used.

2) Program counter (PC)

The PC is made up of a 10-bit counter indicating an immediate address of the program memory (ROM) where the program is stored.

3) Stack register (SR)

The SR is a 10-bit register, storing the contents of the PC plus 1 when the main program calls a subroutine, that is, storing the return address.

4) Program memory (ROM)

The ROM (Read Only Memory) is made up of 16 bits 760 steps, and is used for storing the program.

5) Data memory (RAM)

The RAM (Random Access Memory) is made up of 4 bits 64 words, and is used for storing temporary data.

6) General-purpose register (GR)

The 4 bit $\times$ 16 region of data memory with addresses 00H-0FH is assigned to the general-purpose register to be used in executing instructions.

CIRCUIT DESCRIPTION

7) Arithmetic logic unit (ALU)

The ALU performs binary addition, subtraction, comparison, logical operations, and bit tests.

8) Timer flip-flop (TM F/F)

This flip-flop is set by an 8 Hz signal from the clock generator and reset by a TTM (test timer) command.

9) Timer disable flip-flop (TD F/F)

This flip-flop is set by an 8 Hz signal from the clock generator and reset by a TTM (test timer) command.

10) Unlock flip-flop (UL F/F)

This flip-flop outputs a pulse from the phase detector (ϕ/D) in synchronization with the reference frequency signal (f_r) when PLL is not locked, that is, the divided VCO frequency does not coincide with the reference frequency.

11) Carry flip-flop (C F/F)

This flip-flop is set when a carry or borrow occurs as a result of an arithmetic operation, otherwise it is reset.

12) Judge (J)

This circuit tests the condition of skip instructions.

13) Key

Four key input lines (K0-K3) are provided. A key matrix is formed using 7-bit segment outputs (Sa-Sg) of 5-bit (6-bit) digit outputs D1-D5 (or D1-D6).

14) Segment programmable logic array (SEG PLA)

This array has 5 latched-input bits and 7 output bits, generating a total of 32 segment patterns.

15) Digit programmable logic array (DIG PLA)

This array decodes the digit latch outputs to generate digit outputs D1-D5 and the MT/D6 signal.

16) Reset circuit

The IC device is reset in the following three cases:

1. The power is turned on.
2. The CE line level makes a transition from low to high.
3. The CKSTP instruction has been executed while the CE line is low, and then it gets high.

3. Pulse Swallow system

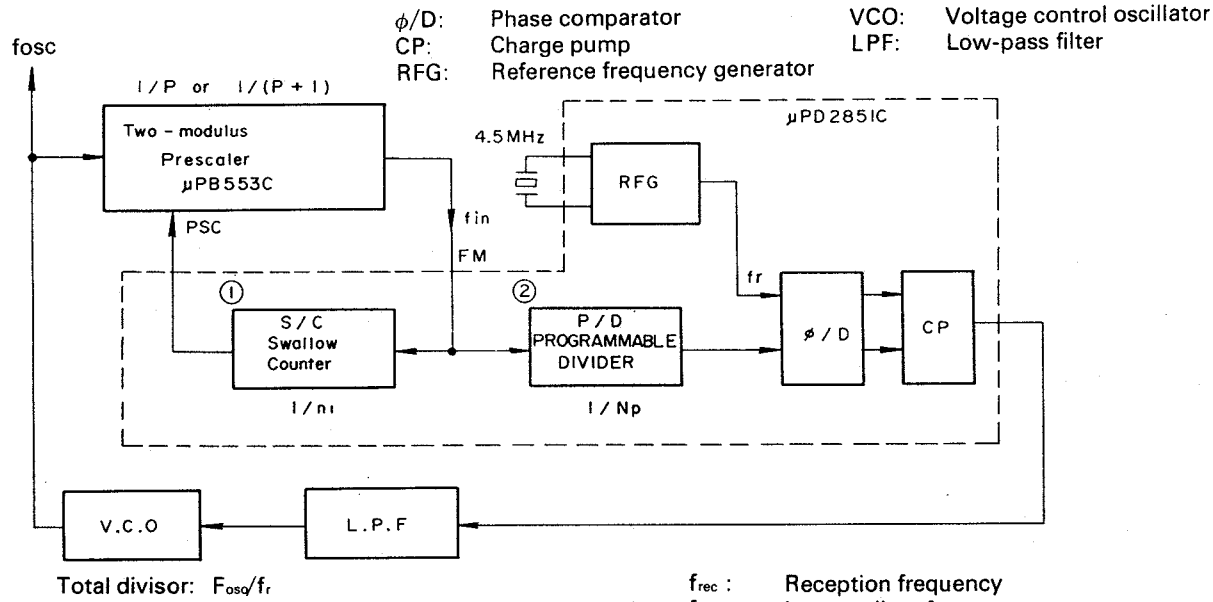
In the PLL system, when the frequency of the VCO increases, the programmable frequency divider which is made up of TTL or MOS devices cannot respond to the operation. One method to solve this problem is the fixed division system in which a prescaler made up of ECL devices is used in the first stage of the programmable divider. Another method is the Pulse Swallow system in which a two-modulus prescaler is used instead of a fixed frequency divider (direct system).

The Pulse Swallow system operates as follows:

1) The dividing ratio is preset in the programmable frequency divider (Swallow counter and programmable counter).
2) The two-modulus prescaler divides the f_{osc} in the 1/(p + 1) division mode until the Swallow Counter becomes 0.

The divided signal is used to count down the Swallow Counter and programmable counter simultaneously.

Block diagram



where, N : Total divisor: F_{osc}/f_r
N_p : Number of "P" and higher figures of N: Divisor of P/D
n_1 : Number of "P" figures
f_r : Reference frequency
f_{osc} : VCO (local osc.) frequency, $f_{osc} = f_{rec} + f_{IF}$
f_{rec} : Reception frequency
f_{IF} : Intermediate frequency
f_{in} : Input frequency on the FM line of μPD2851C, $f_{in} = N_p \cdot f_r$

Fig. 5: NEC μPD2851C + μPB553C Pulse Swallow PLL system

3) When the Swallow counter becomes 0, the two-modulus prescaler enters the 1/p division mode, and the divided signal is used to count down the programmable counter.
4) When the programmable counter becomes 0, the inverted output is sent to the phase detector (ϕ/D). Then, the dividing ratio is preset in the programmable frequency divider, and the same operation is repeated.

The block diagram of this system and the frequency relationship with a frequency table for the FM band in the United States are shown as follows:

Frequency relationship (for U.S. band)

$$fosc = (P + 1)\, n_1 \cdot fr + P(Np - n_1) \cdot fr$$
$$= fr \cdot n_1 + P \cdot Np \cdot fr$$
$$= fr \cdot n_1 + P \cdot fin$$

frec = 87.9 ~ 107.9 MHz (200 kHz Step)
fosc = frec + 10.7 MHz
P = 16
fr = 25 kHz

The following table shows the result of calculations.

Received freq. frec (MHz)	VCO (Local osc. freq.) fosc (MHz)	fin (MHz)	n_1	P/D Divided ratio
87.9	98.6	6.15	8	246
88.1	98.8	6.15	16	246
88.3	99.0	6.15	24	246
88.5	99.2	6.20	0	248
88.7	99.4	6.20	8	248
88.9	99.6	6.20	16	248
89.1	99.8	6.20	24	248
89.3	100.0	6.25	0	250

Table 1: Frequency relationship

Circuit Operation

Control Section

1. AM Switching Circuit

When pin 6 of IC105 is "H", a high output from port Se of IC101 is supplied to port Ko, and IC101 is switched to AM operation. On the other hand, when pin 6 of IC105 is "L", the output signal from port Se is not supplied to Ko, and IC101 is switched to FM operation.

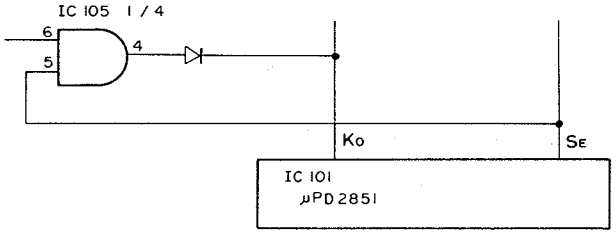


Fig. 6: AM Switching Circuit

2. ABSS (Automatic Broadcasting Sensing System) Operation

1) STAND BY operation and SCAN STOP operation

If the antenna signal becomes weak and the SCAN STOP signal goes off, transistor Q103 turns on and its collector becomes "L".

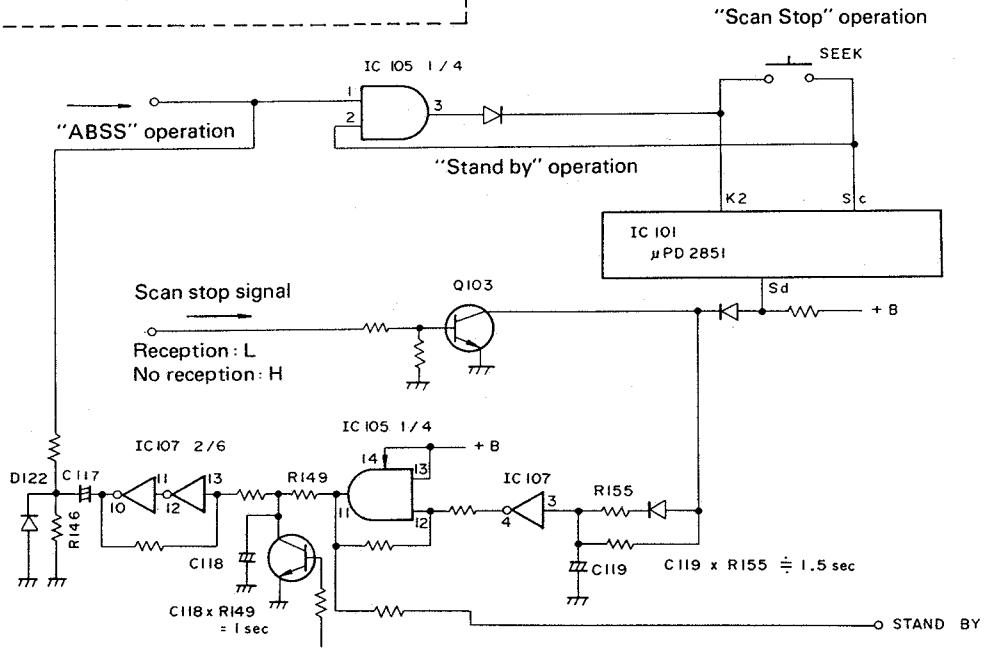


Fig. 7: ABSS operation

CIRCUIT DESCRIPTION

About 4 to 6 seconds after this transition, pin 3 of IC107 becomes "L", pin 4 becomes "H" and the Schmitt-output of IC105 sends out the STAND BY signal at "H" level.

If the cassette deck is in the STAND BY state, the +B power supply to the tuner is shut off and operation is switched to the cassette deck. This is the STAND BY operation in which the cassette deck has priority.

When the cassette deck is not in the STAND BY state, pin 13 of Schmitt trigger IC107 goes to "H" a second after the STAND BY signal. This "H" output is differentiated by C117 and R146, and a positive pulse is applied to pin 1 of IC105. Then an "H" output at pin Sc of IC101 is supplied to the K2 line (pin 23) to activate the SEEK operation, i.e. ABSS operation.

2) SCAN STOP operation

The SCAN STOP terminal receives "H" during SCAN operation and receives "L" when a broadcasting is received. Therefore, transistor Q103 is cut off when a broadcasting is received, port Sd of IC101 becomes "H", then the SCAN operation is stopped.

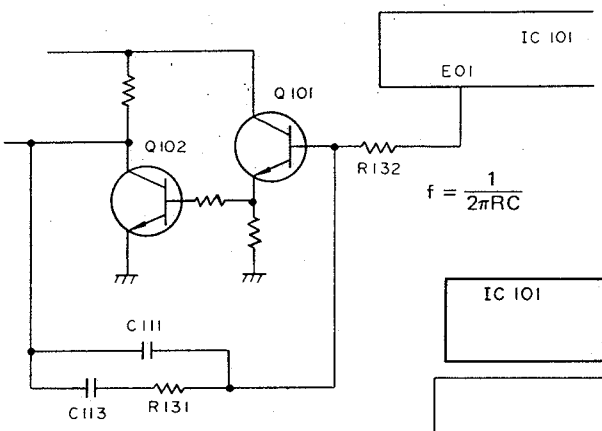


Fig. 8: LPF operation

3. Low Pass Filter (LPF)

Phase error signals detected in IC101 are filtered by the LPF which is made up of Q101 and Q102, in order to cut the high frequency component and convert the signal into a DC voltage which controls the frequency of the VCO.

The characteristics of the LPF is determined by C111, C131, R131, and R132, and the value of these components is eventually determined by the experiment. The damping factor which represents the response of this cirucit is approximately 0.7.

4. Buzzer Circuit

A low-frequency (2 to 5 Hz) and high frequency (2 to 4 kHz) intermittent oscillators are made up of IC106a and IC107a, and IC106b and IC107b, respectively. IC106 also functions as a gate of these oscillators. For instance, when a MUT signal is produced ("H") as a result of key operation, it is transferred through D119 to pin 13 of IC106a, and intermittent oscillations start. The oscillator output is applied to pin 8 of IC106b, and higher-frequency oscillations also start. Eventually, these high and low-frequency intermittent oscillations are combined to drive a ceramic buzzer. IC106c is the gate circuit which activates the buzzer when both pin Sf of IC101 and the D5 line (pin 13) become "H".

D127 is used to prevent buzzer operation when the power is switched off. To do this, the power unit emits a "H" pulse when the power is turned off, and pin 9 of IC107b becomes "H" for a moment, disactivating the oscillators.

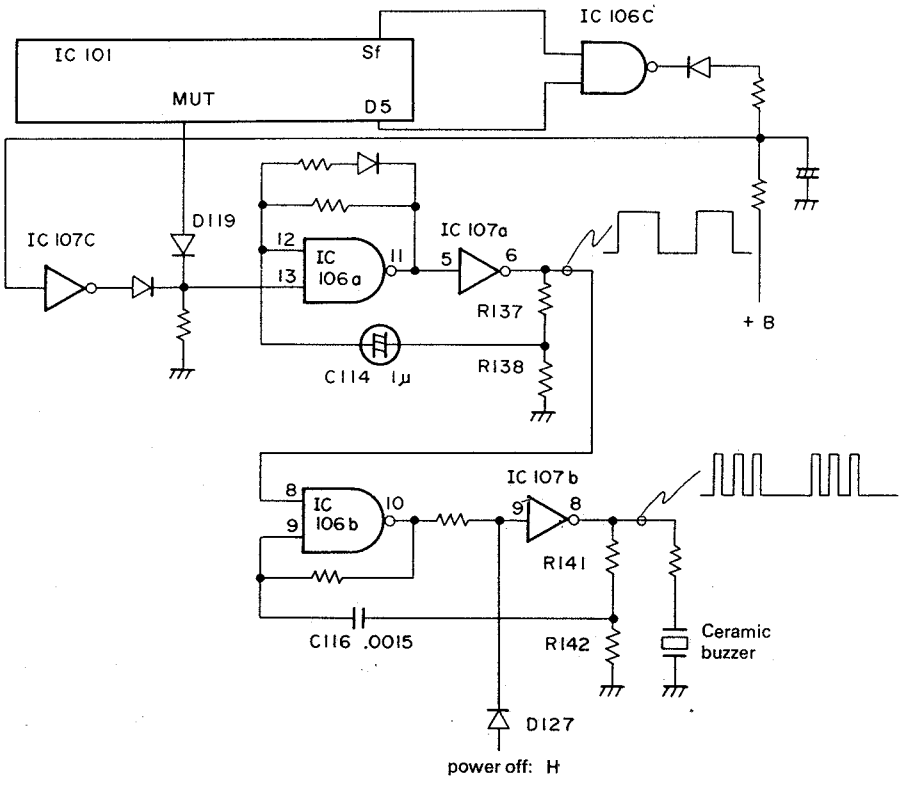


Fig. 9: BUZZER operation

CIRCUIT DESCRIPTION

5. Audio Muting Circuit

When a MUT signal "H" is output from IC101, transistors Q115 and Q116 are turned on so that the audio line is short-circuited. Transistor Q118 is used for muting when the power is turned on and off. While the power is kept off, transistor Q118 maintains the muting signal, since the backup voltage is supplied and the prescaler power supply is turned off. When the power is turned on and the prescaler power voltage is fully built up, the base of Q118 is reversely biased to cut off the transistor and muting is released.

On the other hand, when the power is turned off, only the prescaler power voltage goes off and Q118 turns on simultaneously to perform muting.

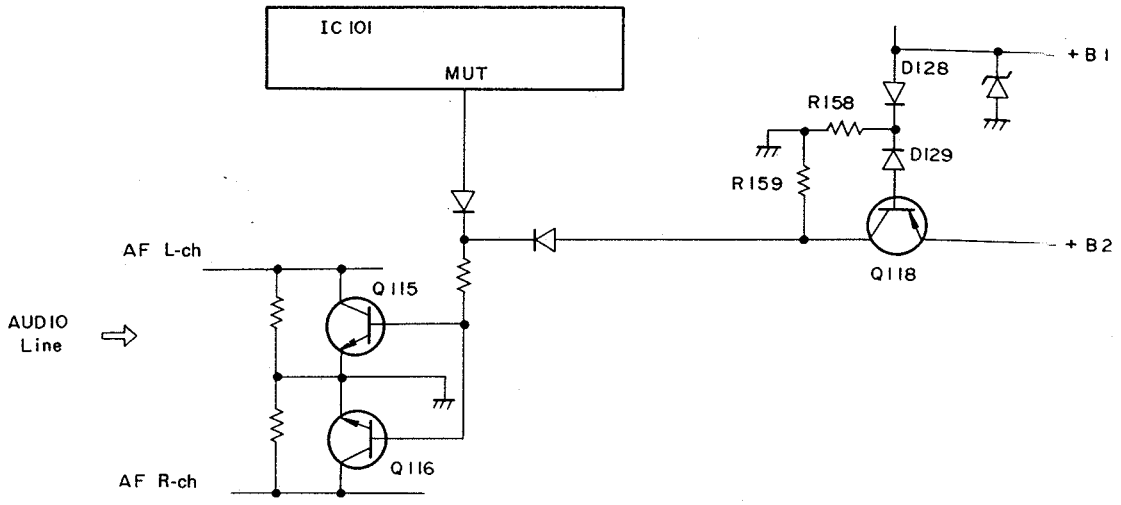


Fig. 10: Audio muting operation

Tuner Section

1. Front End

This is a variable capacitance diode tuner which functions in the same way as a tuner with a single-stage RF amplifier and a 4-section variable capacitor. A silicon N-channel dual gate MOS FET is employed in the RF amplification stage, and it is adapted for a 15 dB AGC with reverse bias at the second gate through the terminal. The tuning variable capacitor diode is of the common cathode type, so that the deviation of tracking is prevented.

2. AM Antenna Circuit

In the case of an AM tuner for a car radio, the rod antenna functions as a capacitor, so it is used as the tuning capacitance in the antenna tuning circuit of a μ-tuning system. Thus, tracking is not deviated when tuning is changed, and high sensitivity can also be obtained. However, in the case of a variable capacitance diode tuner such as this model, it is impossible to tune in the entire band even though one point tuning is possible. Accordingly, the tuning circuit must be independent of the rod antenna. In this KTC-757, FET Q7 separates the RF tuning circuit from the ANT terminal.

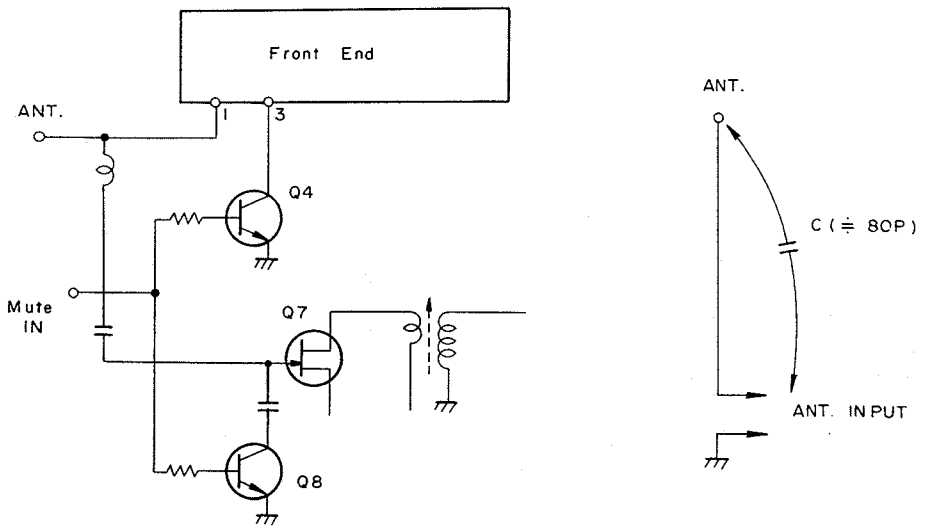


Fig. 11: Front end and antenna operation

CIRCUIT DESCRIPTION

3. SCAN-STOP Signal Generator

1) AM

The IF (450 kHz) signal is amplified by Q9, detected by D9, and then the active low SCAN-STOP signal is produced by Q10.

2) FM

The signal is produced by combining the S-meter signal and muting signal using Q6, D2 and D3. The bandwidth in the muting signal region is ±70 kHz approximately, and it is varied depending on the channel step in each region. When the MODE switch is set at MONO, a positive voltage is applied to the base of Q2, which then turns on to cut the muting signal, and a weak broadcast can be received. At STEREO and ANRC, however, such weak signal is muted.

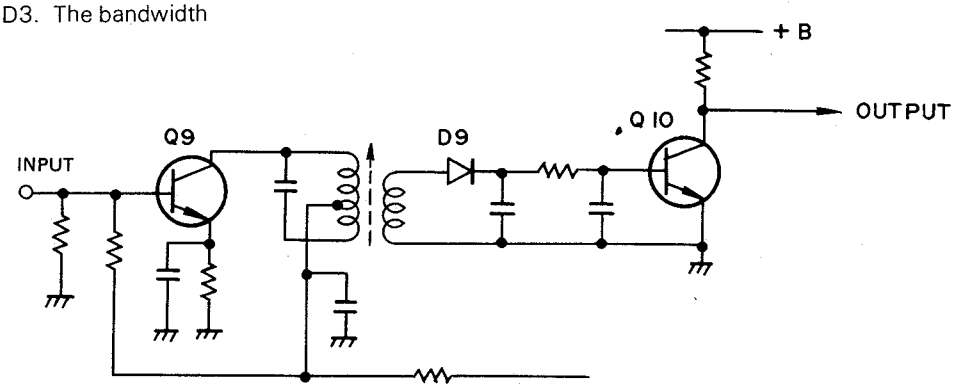


Fig. 12: AM scan stop operation

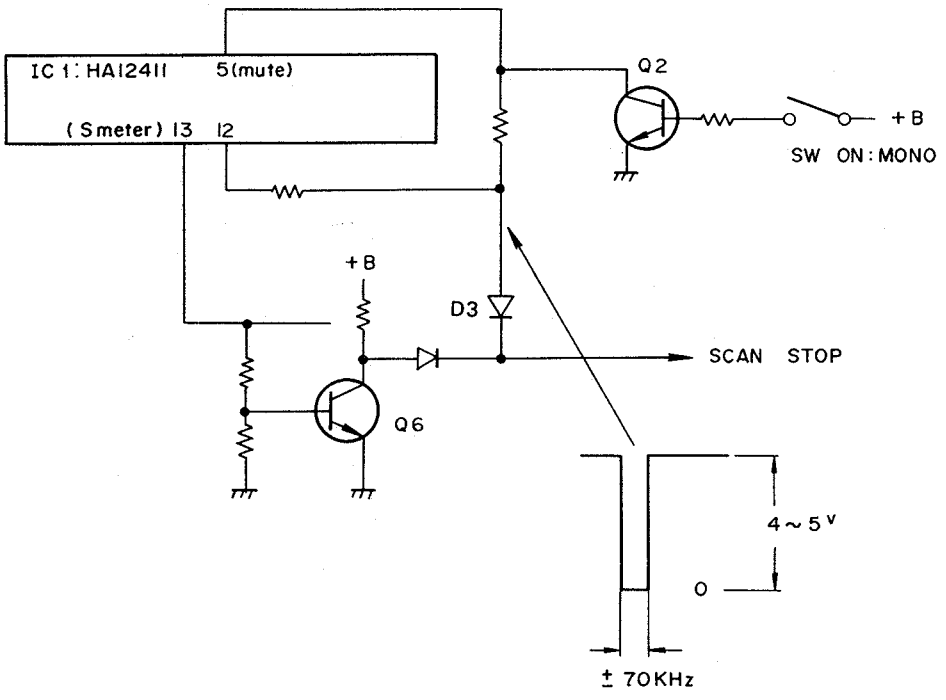


Fig. 13: FM scan stop operation

4. Noise Supressor System

HA11219 (IC2) is a noise suppression circuit specially designed for mobile FM receivers. In this system, this circuit is connected between the quadrature detector and the MPX decoder. This circuit eliminates impulse noise such as ignition noise and wiper noise which have a wide frequency spectrum of more than 100 kHz, to the amount of more than 40 dB peak value.

Circuit operation:

In this mobile FM receiver, the detector output including impulse noise such as ignition noise is supplied to pin 1 . The output signal from pin 2 is filtered by the external high-pass active filter to separate the noise component, and also by the external low-pass active filter to separate the audio signal. The audio signal is sent to the gate circuit through pin 4 . On the other hand, the

CIRCUIT DESCRIPTION

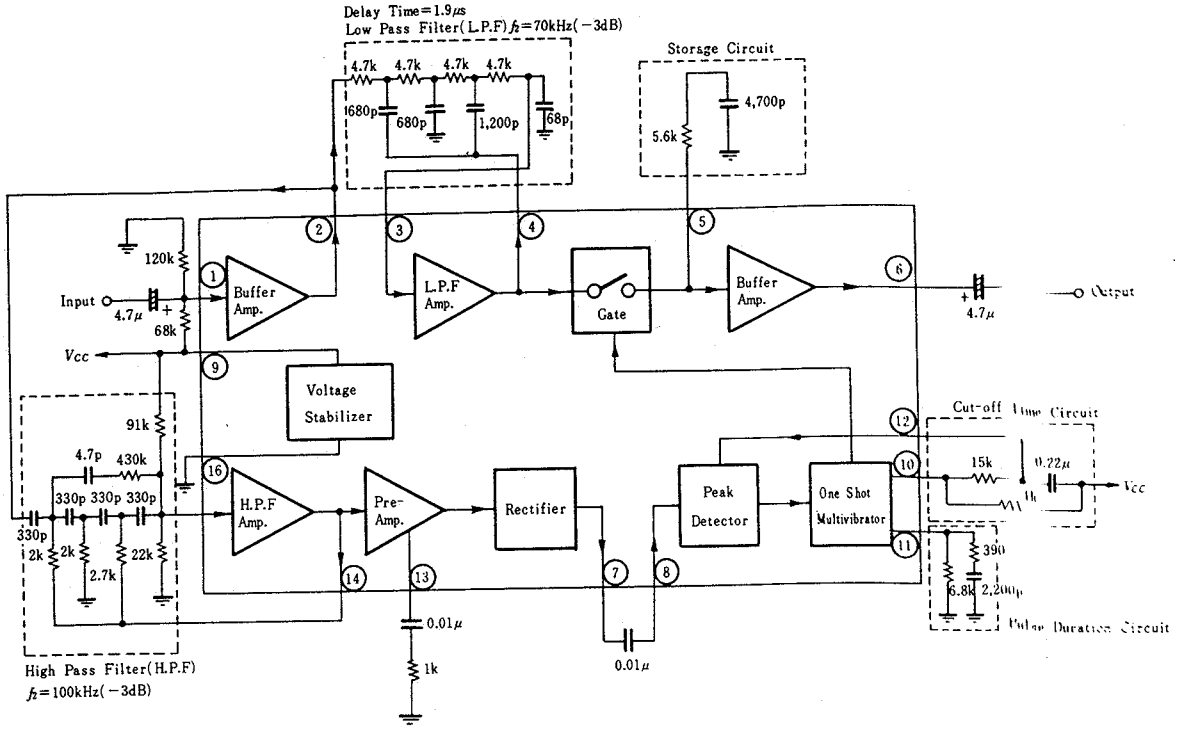


Fig. 14: Schematic of HA11219

noise component is amplified by the pre-amplifier which has the external parameter components at pin 13 to determine the threshold voltage, i.e. the noise sensitivity, and it is sent to the peak detector after being fully rectified.

When the peak value of noise exceeds a certain level, the one-shot multivibrator in the next stage is triggered to generate a gate drive pulse. This gate drive pulse closes the above-mentioned gate circuit for its duration so as to cut the audio signal. Meanwhile, the external hold circuit connected to pin 5 keeps the signal level, so that the audio signal is not interrupted.

The gate-off time, that is, the output pulse width of the one-shot multivibrator is set to 40 μs by external components connected to pin 11 Since ignition noise and wiper noise have a pulse width in the order of 10 μs, most of the impulse noise can be suppressed.

In addition, a Cut Off Time Circuit (COTC) is provided in order to avoid long-term signal interruption due to continuous closing of the gate when the impulse noise comes in consecutively within the time interval of 30 μs. In this case, the COTC forces the gate circuit to open so that the audio signal is conducted, thus noise is not eliminated during this period. The audio signal, from which the impulse noise has been eliminated, is output from pin 6 and sent to the next stage, the MPX demodulator.

5. Pilot Signal Supplementary Circuit

When the Noise Suppressor operates the 19 kHz pilot signal is interrupted, and the MPX circuit does not work for that moment. To rectify this situation, the 19 kHz signal is extracted from the original audio signal at pin 4 , amplified by Q3 to adjust the signal level, and supplied to the MPX circuit.

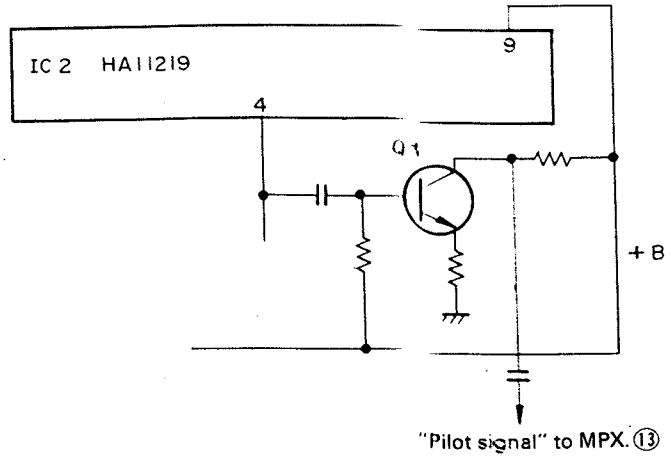


Fig. 15: Pilot signal supplementary circuit

CIRCUIT DESCRIPTION

6. MPX Circuit

KB4448 (IC3) is an FM MPX demodulator especially developed for car radios. It consists of a bipolar monolithic integrated circuit, which incorporates the blending function for reducing the stereo noise particularly with weak signals, in addition to the VCO killer, forced monaural, separation control, and monaural-stereo automatic switching functions. The blending control is carreid out by applying the control voltage from pin 13 of IC1 (FM-IF) to pin 9 (blending control). This is the Automatic Noise Reduction Circuit (ANRC) operation. Forced monaural operation is carried out by applying the +B voltage to pin 12 to deactivate the VCO. Forced stereo operation (ANRC OFF) is carried out by applying the +B voltage to pin 9 , so that the blending operation does not take place. Trimming potentiometers VR1 and VR2 are used to adjust the VCO and stereo separation, respectively.

7. MPX Separation Compensator

In car radio FM reception, MPX separation deteriorates owing to the IF bandwidth and ANRC. This deterioration is compensated by the circuit shown in the figure. The left-channel signal at pin 2 of IC5 is connected to the right-channel signal at pin 8 through a common impedance R70 for blending, so that crosstalk is cancelled. The amount of blending depends upon R70, the value of which is determined in consideration of the adjustment range of VR2 in the MPX circuit.

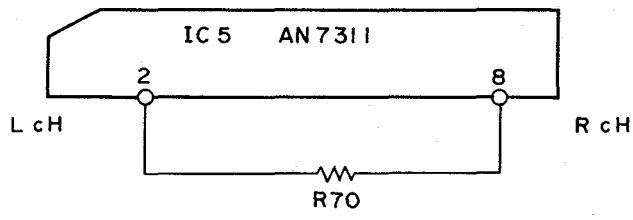


Fig. 17: Separation Compensator

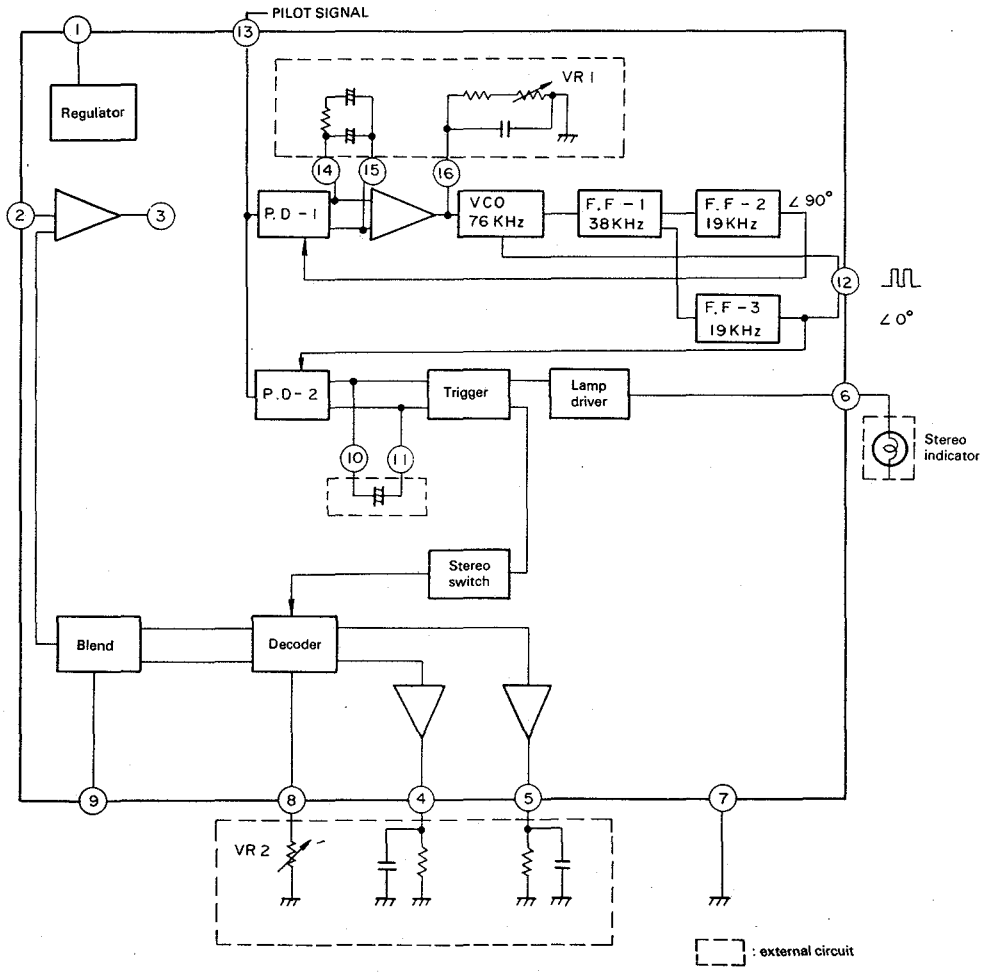


Fig. 16: Schematic of KB4448